ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-103

PHYSICAL LAYER AT THE BASIC ACCESS INTERFACE BETWEEN DATA PROCESSING EQUIPMENT AND PRIVATE SWITCHING NETWORKS

2nd Edition – December 1987

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BRIEF HISTORY

This Standard ECMA-103 is one of a series of standards for the connection of data processing equipment to private switching networks.

It uses the ISDN concepts as developed by CCITT and it is also within the framework of standards for open systems interconnection as defined by ISO 7498 and within the Technical Report ECMA TR/24. It is based on the practical experience of ECMA member companies and the results of their active and continuous participation in the work of ISO, CCITT and various national standardization bodies in Europe and in the USA. It represents a pragmatic and widely based consensus.

The Standard ECMA-103 defines the Physical Layer of the interface as presented by the data processing equipment. Where appropriate, assumptions on the interface as presented by the private circuit switching network are also indicated.

The second edition has been adapted to CCITT Rec. I.430 as approved by the Accelerated Procedure in 1987.

Accepted as Standard ECMA-103, 2nd Edition, by the General Assembly of ECMA of 10th December 1987.

TABLE OF CONTENTS

1. SCOPE AND FIELD OF APPLICATION

This ECMA Standard specifies the Physical Layer characteristics of the basic access interface between data processing equipment (DPE) and private switching networks (PSN), and is based on CCITT Rec. I.430. The interface concerned is at the S reference point as defined in CCITT Rec. I.411. The reference configuration for the interface is given in Figure 1.

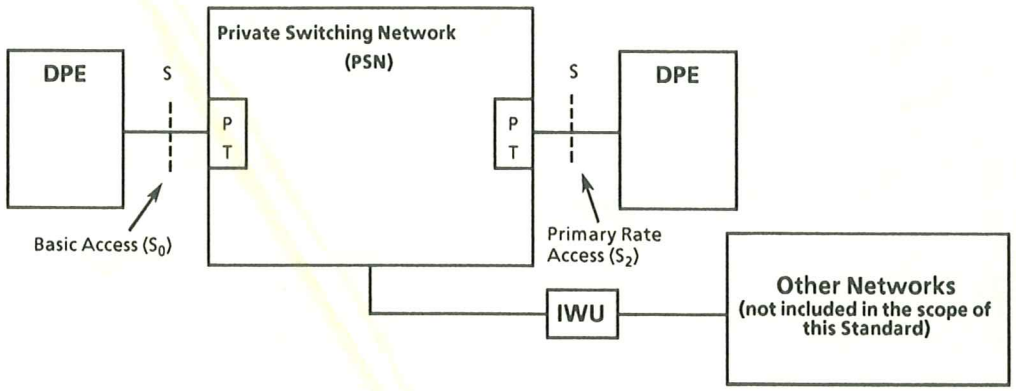


Figure 1 - Reference Configuration showing S_0 and S_2 Interfaces

2. REFERENCES

ECMA-83	Safety Requirements for DTE-to-DCE Interface in Public Data Networks
ECMA-105	Data Link Layer Protocol between Data Processing Equipment and Private Switching Networks
ECMA TR/35	Safety Requirements for Equipment to be connected to Telecommunication Networks
CCITT Rec. G.117	Transmission aspects of unbalance about earth (definitions and method)
CCITT Rec. I.112	Vocabulary of terms for ISDNs
CCITT Rec. I.320	ISDN protocol reference model
CCITT Rec. I.411	ISDN user-network interfaces - reference configurations
CCITT Rec. I.412	ISDN user-network interfaces - interface structures and access capabilities
CCITT Rec. I.430	Basic user-network interface - layer 1 specification
CCITT Rec. O.121	Measuring arrangements to assess the degree of unbalance about earth

CCITT Rec. V.52	Characteristics of distortion and error-rate measuring apparatus for data transmission
CCITT Rec. V.57	Comprehensive data test set for high data signalling rates
CCITT Rec. X.200	Reference model of Open Systems Interconnection for CCITT applications
CCITT Rec. X.211	Physical layer service definitions of open system interconnections for CCITT applications
CCITT Rec. Z.101..104	Recommendations on the functional specification and description language (SDL)

Note 1

For the CCITT Recommendations listed above (except I.430) the Red Book versions apply. The reference for CCITT Rec. I.430 can be found in report COM. XVIII R21 C.

ISO 7498	Open Systems Interconnection - Basic Reference Model
ISO DIS 8877	Information Processing Systems-Interface connector and contact assignment for ISDN basic access interface located at reference points S and T.

3. DEFINITIONS

A basic vocabulary of terms can be found in CCITT Rec. I.112. In addition, the following definitions apply in this Standard:

3.1 B-Channel

A 64 kbit/s access channel with bit and octet timing used to carry user data in both directions of transmission between DPEs connected over a PSN.

3.2 D-Channel

A 16 kbit/s access channel used to carry signalling and other information in both directions of transmission between a DPE and the PSN.

3.3 Data Processing Equipment (DPE)

Specific type of terminal equipment, exclusively or mainly used to process data (in contrast to a voice-only terminal).

3.4 Interworking Unit (IWU)

The functional block needed for a PSN to interwork with other networks.

3.5 Layer Service

This term is defined in the ISO Reference Model on Open Systems Interconnections (ISO 7498).

3.6 Private Switching Network (PSN)

A private ISDN providing circuit and/or packet/frame switching functions. It is operated by the user and located on his premises to cover the communications needs in his domain. Data processing equipment is connected to a PCSN at its S reference points.

3.7 PSN Termination (PT)

The termination of a PSN at the S reference point.

3.8 S_0 Interface

The basic access interface at the S reference point (see CCITT Rec. I.411) operating at a physical bit rate of 192 kbit/s. It provides access to two B-channels and one D-channel (2B + D). The S_0 interface forms one of the user access points to a PSN.

3.9 S_2 Interface

The primary rate access interface at the S reference point (see CCITT Rec. I.411) operating at a physical bit rate of 2048 kbit/s. It provides access to 30 B-channels and one D-channel (30B + D). The S_2 interface forms one of the user access points to a PSN.

3.10 Specification and Description Language (SDL)

The specification and description language according to CCITT Rec. Z.101 to Z.104.

3.11 Terminal Equipment (TE)

A general term to designate any terminal (voice or data processing or combination of both) connected to a PSN at the S_0 or at the S_2 interface.

4. LAYER SERVICE CHARACTERISTICS

General information on layer services and layered protocols can be found in CCITT Rec. X.200 and ISO 7498.

4.1 Layer Services required from the Physical Medium

The Physical Layer of this interface requires a balanced metallic transmission medium for each direction of transmission, capable of supporting 192 kbit/s.

4.2 Layer Services provided to the Data Link Layer

The Physical Layer shall provide the following layer services to the Data Link Layer:

- Transmission capability by means of appropriately encoded bitstreams, for both B-channels and the D-channel.
- Timing and synchronization functions.
- The signalling capability and the necessary procedures to enable user terminals and/or network terminating equipment to be activated and deactivated. The activation and deactivation procedures are defined in 8.2.

- The signalling capability and the necessary procedures to allow terminals to gain access to the common resource of the D-channel in an orderly fashion, while meeting the performance requirements of the D-channel signalling systems. These D-channel access control procedures are defined in 8.1.
- The signalling capability and procedures and the necessary functions to enable the maintenance functions to be performed.
- An indication to the higher layers and the Management Entity about the status of the Physical Layer.

4.3 Primitives between the Physical Layer and other Entities

- The primitives used between the Physical Layer and other entities are:

PH-AI/AR, MPH-AI/AR	see 8.2.1.4
PH-DI, MPH-DI/DR	see 8.2.1.5
MPH-EI/ES	see 8.2.1.6
MPH-II	see 8.2.1.7
PH-DATA-I/R	PHYSICAL LAYER DATA INDICATION/ REQUEST

These primitives are used to indicate the arrival of a message unit or to request that a message unit be sent.

- The primitives represent the logical exchange of information and control between the Physical Layer, the Data Link Layer and the Management Entity, see Figure 2. They do not specify nor constrain the implementation of entities or interfaces. For a description of the syntax and use of the primitives refer to CCITT Rec. X.211.

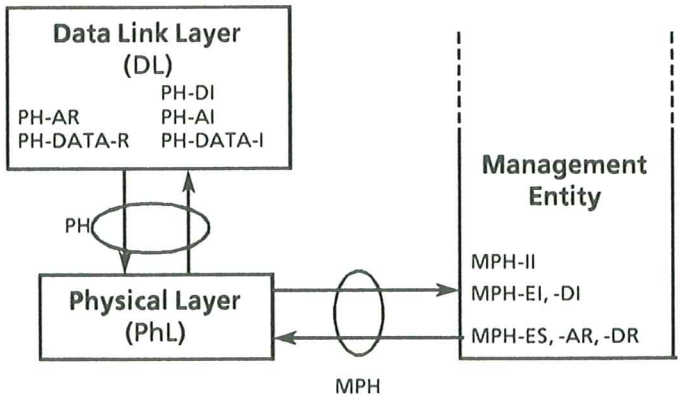


Figure 2 - Physical Layer Primitives

- The values of the primitives are defined in Table 1. Relevant detailed description of the primitives and their procedures are given in 8.2.1.

Generic Name	Function		Parameter		Message Unit Contents	
	Request	Indica-tion	Priority Indicator	Message Unit		
PH-DATA	x Note 2	x	x Note 3	x	Data Link Layer peer-to-peer message	↑ between Phy-sical and Data Link Layer ↓
PH-ACTIVATE	x	x	–	–		
PH-DEACTIVATE	–	x	–	–		
MPH-ACTIVATE	x	x	–	–		↑ between Physical Layer and Management Entity ↓
MPH-DEACTIVATE	x	x	–	x		
MPH-ERROR	–	x Note 4	–	x	Note 4	
MPH-INFORMATION	–	x	–	x	Connected / Disconnected	

Table 1 - Values of Physical Layer Primitives

Note 2

PH-DATA-REQUEST implies underlying negotiation between the Physical and the Data Link Layer for the acceptance of the data.

Note 3

Priority indication applies only to the REQUEST type.

Note 4

The indication includes the type of error or recovery from a previously reported erroneous situation.

5. MODES OF OPERATION

The characteristics of the Physical Layer interface shall allow for point-to-point and point-to-multipoint modes of operation. The mode of operation used at the Physical Layer shall not affect the procedures at higher layers.

5.1 Point-to-Point Operation

Point-to-point operation at the Physical Layer shall imply that only one source (sender) and one sink (receiver) are active at the interface at any one time in each direction of transmission. Such operation shall be independent of the number of connectors which may be provided on a particular wiring configuration (see 6).

5.2 Point-to-Multipoint Operation

Point-to-multipoint operation at the Physical Layer shall allow more than one terminal (source and sink pair) to be simultaneously active at an S reference point. The multipoint mode of operation may be accommodated, as discussed in 6, with point-to-point or point-to-multipoint wiring configurations.

6. TYPES OF WIRING CONFIGURATION

Figure 3 shows general reference configurations for the wiring at user premises. The electrical characteristics of the S_0 interface are determined on the basis of certain assumptions about the various wiring configurations which may exist within users' premises. These assumptions are identified in the configuration descriptions of Figure 3.

6.1 Point-to-Point Configuration

Point-to-point wiring configuration shall imply that only one source (sender) and one sink (receiver) are interconnected via an interchange circuit.

6.2 Point-to-Multipoint Configuration

Point-to-multipoint wiring configurations shall allow more than one source to be connected to the same sink or more than one sink to be connected to the same source via an interchange circuit. Such distribution systems are called "passive busses" and are characterized by the fact that they contain no active logic elements.

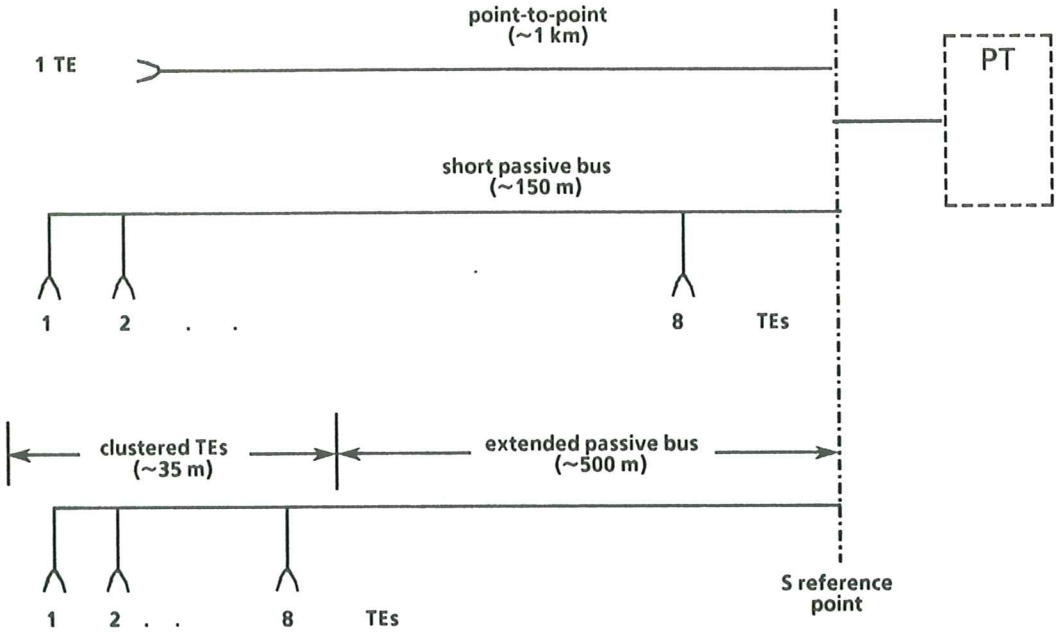


Figure 3 - Reference Configurations for Basic Access Wiring at the User's Premises

Note 5

The lengths depend on the electrical characteristics of the cabling and the values indicated are given for tutorial background information only.

6.3 Wiring Polarity Integrity

For a point-to-point wiring configuration the two wires of the interchange circuit pair may be reversed. However for point-to-multipoint wiring configurations, the

wiring polarity integrity of the interchange circuit from the TEs to the PT shall be maintained between the TEs.

6.4 Location of the Interfaces

The wiring on the user's premises shall be considered to be one continuous cable run with sockets for the TE attached directly to the cable or using stubs of shorter than 1 m. The socket and the wiring on the user's premises are beyond the scope of this Standard, see Figure 4.

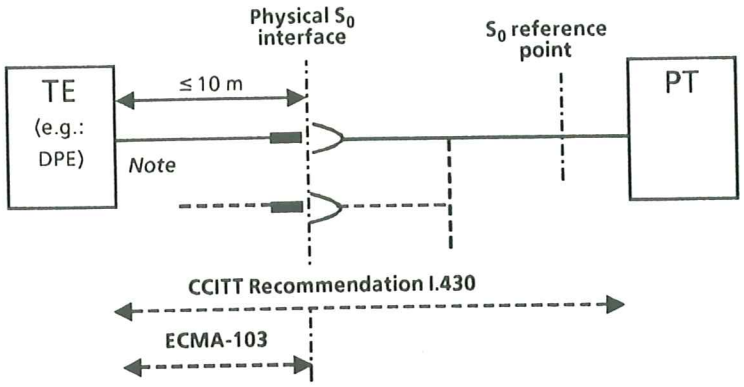


Figure 4 - Location of the S_0 Interface

Note 6

The connection cord may be detachable.

6.5 DPE associated Wiring

The wiring between DPE and its associate socket can affect the electrical characteristics of the interface. A DPE may be equipped with either of the following means for connection to the interface point:

- a hard-wired connection cord of not more than 10 m and a connector as specified in 12.1, or
- a socket with a connection cord of not more than 10 m, which has a connector as specified in 12.1, at each end.

Although a DPE may be provided with a cord of less than 5 m, it shall meet the requirements of this Standard with a cord having a minimum length of 5 m. Such a cord may be provided as part of the DPE, or the DPE may be designed to conform to the electrical characteristics specified in 10 with a "standard ISDN basic access TE cord" conforming to the requirements specified in 10.9 and having the maximum permitted capacitance.

7. FUNCTIONAL CHARACTERISTICS

7.1 Interface Functions

7.1.1 Bit Timing

This function shall provide bit (signal element) timing at 192 kbit/s to enable DPE and PT to recover information from the aggregate bit stream.

7.1.2 Octet Timing

This function shall provide 8 kHz octet timing for the PT and DPE.

7.1.3 Frame Alignment

This function shall provide information to enable PT and DPE to recover the time division multiplexed channels.

7.1.4 B-Channel

This function shall provide two independent access channels each having a bit rate of 64 kbit/s for each direction of transmission, as defined in CCITT Rec. I.412.

7.1.5 D-Channel

This function shall provide an access channel with a bit rate of 16 kbit/s for each direction of transmission, as defined in CCITT Rec. I.412.

7.1.6 D-Channel Access Procedure

This function shall enable terminals to gain access to the common resource of the D-channel in an orderly controlled fashion. The functions necessary for these procedures shall include an echoed D-channel at a bit rate 16 kbit/s in the direction PT to DPE. For the definition of the procedures relating to D-channel access, see 8.1.

7.1.7 Power Feeding

This function shall provide for the capability to transfer power across the interface from the PSN (PT) to the DPE. The detailed specification of the power feeding function is given in 11.

7.1.8 Deactivation

This function shall permit the DPE to be placed in a lower power consumption mode, e.g. when no call is in progress. The procedures and precise conditions under which deactivation takes place are specified in 8.2.

7.1.9 Activation

This function shall allow DPE and PT to be restored to their normal operating power mode. The procedures and precise conditions under which such deactivation takes place are specified in 8.2.

7.2 Interchange Circuits

Two interchange circuits, one for each direction of transmission, shall be used to transfer digital signals across the interface. All functions described in 7.1, except for power feeding, shall be carried by means of a digitally multiplexed signal structured as defined in 7.4.

7.3 Connected/Disconnected Indication

The appearance/disappearance of power shall be the criterion used by the DPE to determine whether it is connected/disconnected.

A terminal powered across the interface shall consider itself connected when it detects the presence of power.

A terminal not powered across the interface may consider itself disconnected either if it can detect the disappearance of voltage from power source 1 (when provided; see 11) or on absence of local power.

The indication, that the terminal is disconnected, shall be sent to the Management Entity by means of the MPH-Error Indication primitive.

7.4 Frame Structure

In both directions of transmissions, the bits shall be grouped into frames of 48 bits each. The frame structure shall be identical for point-to-point and point-to-multipoint configurations.

7.4.1 Bit Rate

The nominal transmitted bit rate at the interface shall be 192 kbit/s in both directions of transmission.

7.4.2 Binary Organization of the Frame

The frame structures are different for each direction of transmission. Both structures are illustrated in Figure 5.

7.4.2.1 DPE to PSN

Each frame shall consist of the following groups of bits, each individual group being DC-balanced by a trailing bit (L-bit):

Bit Position	Group
1 - 2	F and L-bit (framing and balance bits)
3 - 11	B1-channel with balance bit (first octet)
12 - 13	D and L-bit (D-channel bit with balance bit)
14 - 15	F_A or Q and L-bit (auxiliary framing and balance bits)
16 - 24	B2-channel with balance bit (first octet)
25 - 26	D and L-bit (D-channel bit with balance bit)
27 - 35	B1-channel with balance bit (second octet)
36 - 37	D and L-bit (D-channel bit with balance bit)
38 - 46	B2-channel with balance bit (second octet)
47 - 48	D and L-bit (D-channel bit with balance bit)

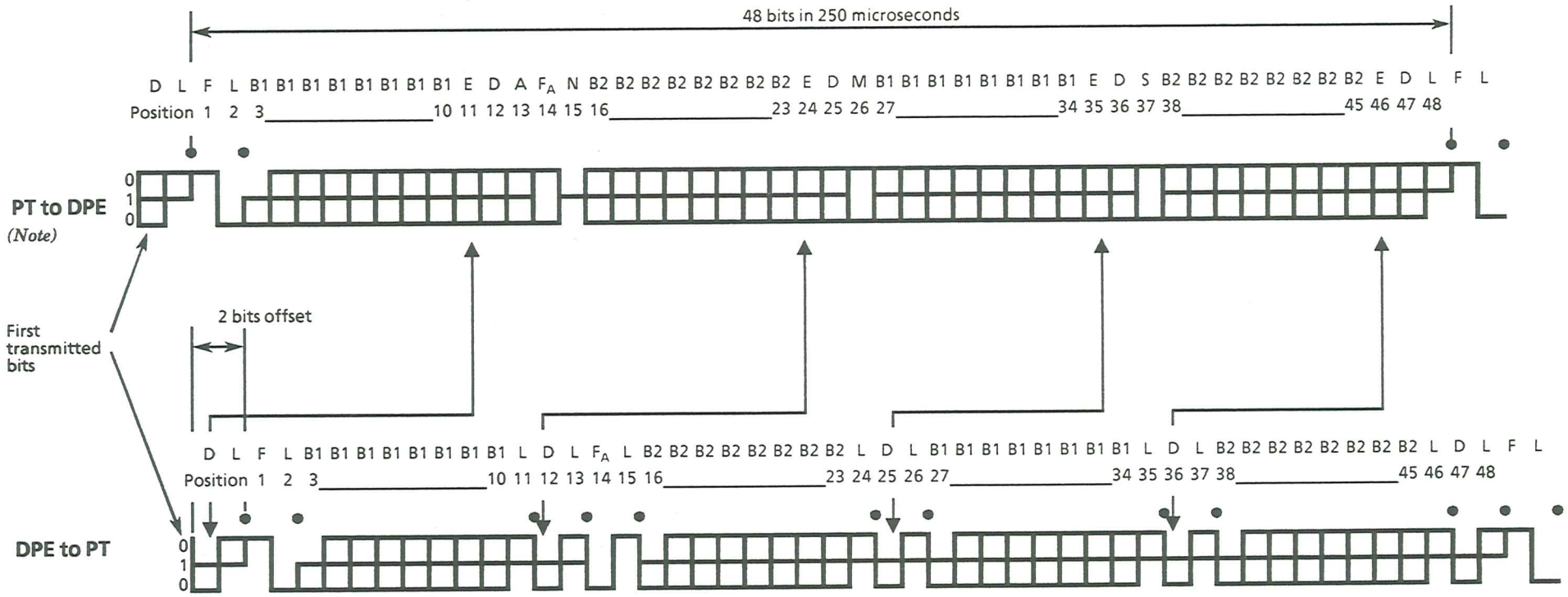
7.4.2.2 PSN to DPE

Frames transmitted by the PSN shall contain a D-echo channel (E-bits) used to re-transmit the D-bits received from the terminals. The D-echo channel shall be used for D-channel access control. The last bit of the frame (L-bit) shall be used for balancing each complete frame. The bits are grouped as follows:

Bit Position	**Group**
1 - 2	F and L-bits (framing and balance bits)
3 - 10	B1-channel (first octet)
11	E-bit (D-Echo-channel bit)
12	D-channel bit
13	A-bit used for activation
14	F_A-bit (auxiliary framing bit)
15	N-bit (coded as defined in Figure 5)
16 - 23	B2-channel (first octet)
24	E-bit (D-Echo-channel bit)
25	D-channel bit
26	M-bit (multi-framing bit)
27 - 34	B1-channel (second octet)
35	E-bit (D-Echo-channel bit)
36	D-channel bit
37	S-bit (reserved for future standardization)
38 - 45	B2-channel (second octet)
46	E-bit (D-Echo-channel bit)
47	D-channel bit
48	L-bit (frame balance bit)

Note 7

The S-bit shall be always set to ZERO.



Legend:

F	=	Framing bit
L	=	DC balancing bit
D	=	D-channel bit
E	=	D-echo-channel bit
F_A	=	Auxiliary framing bit (= 0). If the Q-channel capability is employed, bit position 14 of the direction DPE to PT will carry a Q-bit in every fifth frame.
N	=	bit set to a binary value N = NOT(F_A)
B1	=	bit within B-channel 1
B2	=	bit within B-channel 2
A	=	bit used for activation
S	=	reserved for future standardization
•	=	Dots mark the boundaries of those parts of the frame that are independently DC-balanced.
M	=	Multiframing bit

Note:
Due to possible reversion of the two wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

Figure 5 - Frame Organization

Note 8

Due to possible reversion of the two wire interchange circuits (see 6.3), the bits may be received with opposite polarity.

7.4.2.3 Relative Bit Positions

At the terminals, timing in the direction DPE to PT shall be derived from the frames received from the PT.

The first bit of each frame transmitted from a DPE towards the PT shall be offset by two bit periods with respect to the first bit of the frame received from the PT. Figure 5 illustrates the relative bit positions for both transmitted and received frames.

7.5 Line Code

For both directions of transmission pseudo-ternary coding is used with 100% pulse width as shown in Figure 6. Coding shall be such that a ONE is represented by no signal voltage applied to the line, and a ZERO is represented by a positive or negative voltage, i.e. a positive or negative pulse. Consecutive ZEROs shall be represented by pulses of opposite voltage.

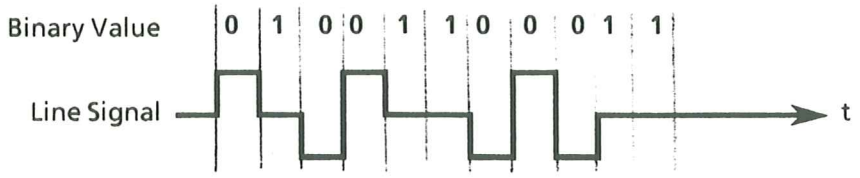


Figure 6 - Pseudo-Ternary Code (Example)

The framing bit (bit 1, "F") shall always be transmitted as a positive pulse. The balance bit (bit 2, "L") immediately following the framing bit shall be of opposite polarity.

The first ZERO following bit 2 shall be of the same polarity as bit 2. Subsequent ZEROs shall alternate in polarity. A balance bit shall be set to ZERO if the number of ZEROs following the last balance bit is odd. It shall be set to ONE if the number of ZEROs following the last balance bit is even.

Note 9

Due to possible reversion of the two wire interchange circuits (see 6.3), the bits may be received with opposite polarity.

7.6 Timing Considerations

A DPE shall synchronize its timing (bit, octet, frame) to the signal received from the PSN ans use this derived timing to synchronize its transmitted signal.

8. INTERFACE PROCEDURES

General information on interface procedures and layered protocols can be found in CCITT Rec. X.200 and Standard ISO 7498. The subsequent paragraphs describe the detailed procedures at the Physical Layer interfaces to the Data Link Layer and to the Management Entity.

8.1 D-Channel Access Procedure

The following procedure shall allow a number of terminals, being part of a multi-point configuration, to gain access to the D-channel in an orderly fashion. The procedure shall ensure that, even in cases where two or more terminals attempt to access the D-channel simultaneously, one terminal will always be successful in completing transmission of its information. This procedure relies upon the use of the Data Link Layer frames delimited by flags consisting of the binary pattern 01111110 and the technique of insertion of ZEROs to prevent flag imitation; see Standard ECMA-105.

The D-channel access procedure shall also permit terminals to operate in a point-to-point manner.

8.1.1 Interframe Time Fill

When a DPE or PT has no Data Link Layer frames to transmit, it shall send ONEs on the D-channel.

8.1.2 D-Echo Channel

On receipt of a D-channel bit from the DPE(s), the PT shall reflect its binary value in the next available D-echo channel bit position towards the DPE(s).

8.1.3 D-Channel Monitoring

In the ACTIVATED state (see 8.2) the DPE shall monitor the D-echo channel and count the number of consecutive ONEs. If a ZERO is detected, the terminal shall restart counting the number of consecutive ONEs. The current value of the count is called C. It need not be incremented after the decimal value 11 has been reached.

8.1.4 Priority Mechanism

The Data Link Layer frames shall be transmitted so that signalling information is given priority (priority class 1) over all other types of information (priority class 2). Furthermore, to ensure that within each priority class all competing DPEs are given a fair chance to access the D-channel, once a DPE has successfully completed the transmission of a frame it shall be given a lower level of priority within that class. The terminal is given back its normal level within a priority class when all terminals have had an opportunity to transmit information at the normal level within that priority class.

The priority class shall be passed down from the Data Link Layer as a parameter of the PH-DATA-REQUEST primitive.

The priority mechanism is based on the requirement that a terminal may only start the Data Link Layer frame transmission when C (see 8.1.3) equals, or exceeds, the value X_1 for priority class 1 or equals, or exceeds, the value X_2 for priority class 2. The value X_1 shall be 8 for the normal level and 9 for the lower level of priority. The value X_2 shall be 10 for the normal level and 11 for the lower level of priority.

In either priority class, the value of the normal level of priority shall be changed into the value of the lower level of priority when a terminal has successfully transmitted a Data Link Layer frame of that priority class.

The value of the lower level of priority shall be changed back to the value of the normal level of priority when C (see 8.1.3) equals the value of the lower level of priority.

8.1.5 Collision Detection

While transmitting information in the D-channel the terminal shall monitor the received D-echo channel bit and compare the last transmitted bit with the next available D-echo bit. If the transmitted bit is the same as the received echo, the terminal shall continue its transmission. If however, the received echo is different from the transmitted bit the terminal shall cease transmission immediately and return to the D-channel monitoring state.

8.1.6 Access Control Procedure

Figure 7 shows the SDL diagram of the D-channel access procedure. The following variables are used in the SDL diagram:

C	=	Count of E-bits received as ONEs
D	=	Value of the most recently transmitted D-channel bit (D-bit)
i	=	Priority class of the message to be transmitted (either "1" or "2")
E	=	Value of the most recent D-echo channel bit
X_1	=	Number of consecutive E-bits to be received as ONEs before transmitting a message of priority class 1
X_2	=	Number of consecutive E-bits to be received as ONEs before transmitting a message of priority class 2
X_i	=	Either X_1 or X_2 according to the value of "i"
Y	=	Binary variable indicating that the frame is pending

The SDL diagram does not cover the queuing functions which are necessary when a second DATA-REQUEST is received before the first message unit has been transmitted.

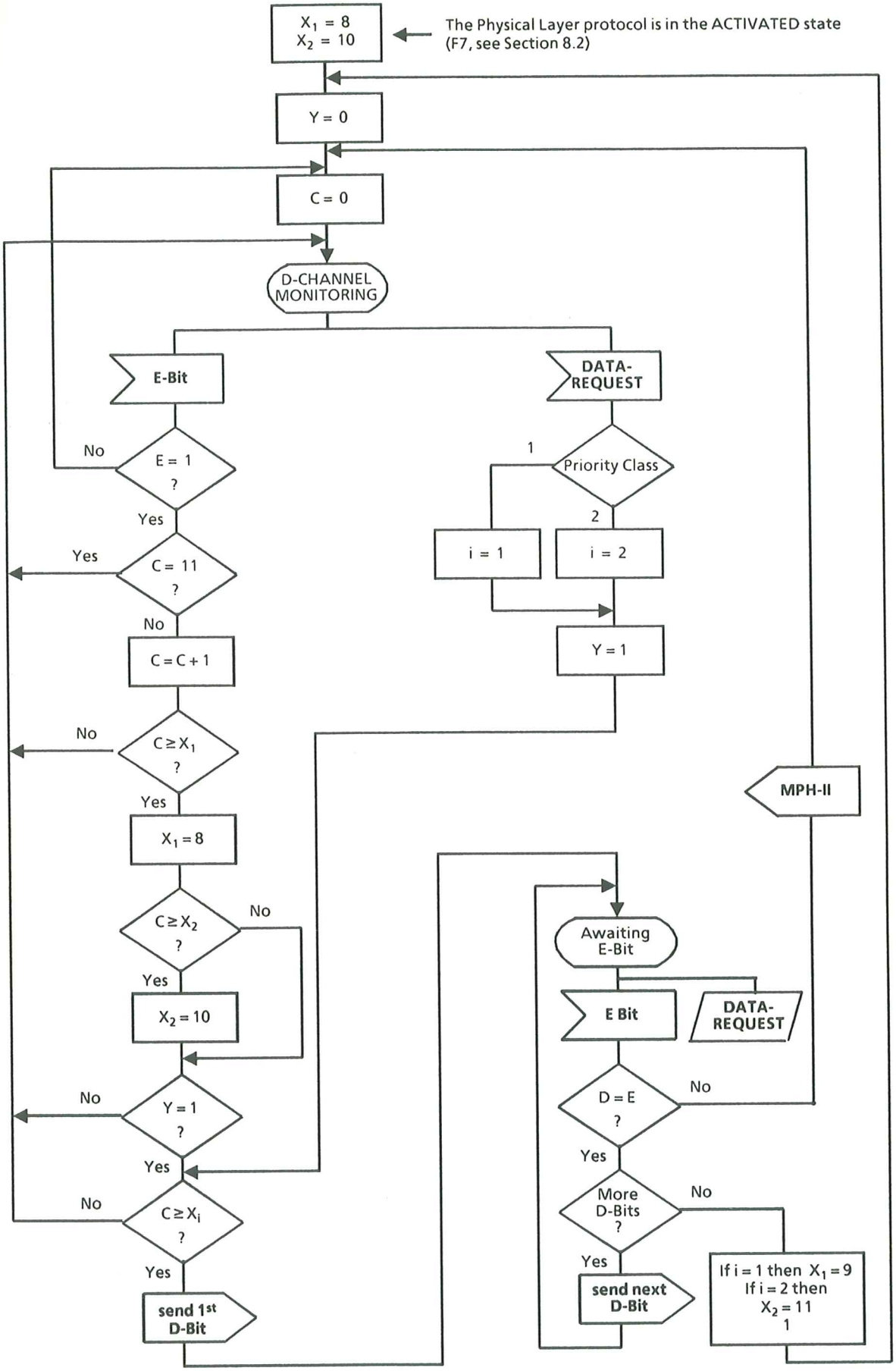


Figure 7 - SDL Presentation of the D-Channel Access Procedure

8.2 Activation/Deactivation

8.2.1 Definitions

8.2.1.1 Signals

The designation, the meaning and the coding of the Physical Layer signals across the S reference point are given in Table 2.

Signals from the PSN to the DPE		Signals from the DPE to the PSN	
INFO 0	Transmission of continuous binary ONEs Note 11 INFO 0 is only recognized by the DPE when it has lasted for longer than 250 µs.	INFO 0	Transmission of continuous binary ONEs Note 11 INFO 0 is not recognized by the PCSN until it has lasted for longer than 15 ms Note 12
		INFO 1	A signal requesting activation, consisting of the continuous transmission of the following pattern: Positive ZERO, negative ZERO, six ONEs Nominal bit rate = 192 kbit/s Note 13
INFO 2	A signal to allow synchronization to the PCSN clock, consisting of frames with all bits of the B-, D- and D-Echo channels, set to binary ZERO, the A-bit set to ZERO, the N- and L-bits set according to the normal coding rules Note 14		
		INFO 3	A signal indicating the SYNCHRONIZED or the ACTIVATED state, consisting of synchronized frames with operational data on the B- and D-channels.
INFO 4	A signal indicating the ACTIVATED state, consisting of frames with operational data on the B-, D- and D-echo channels; the A-bit is set to ONE Note 14		

Table 2 - Definition of Physical Layer Signals *(Note 10)*

Note 10

With configurations where the wiring polarity may be reversed, signals may be received with the polarity of the ZEROs inverted.

Note 11

This value ensures that the PSN remains in the ACTIVATED state while the DPE is recovering from the LOST FRAMING state.

Note 12

For the coding of ONEs and ZEROs see 7.5.

Note 13

DPEs which do not need the capability to initiate the activation of an inactivated interface (i.e. DPEs designed to handle incoming calls only) need not have the capability to send INFO 1.

Note 14

During transmission of INFO 2 or INFO 4, the F_A bits and the M-bits from the PT may provide the Q-bit pattern designation as described in 8.5.

8.2.1.2 DPE States

The DPE states shall be as follows:

F1 INACTIVE	The DPE is not powered on.
F2 SENSING	The DPE is powered on, but has not determined the type of signal, if any, that it is receiving.
F3 DEACTIVATED	The DPE is in the idle state, i.e. it is neither transmitting nor receiving a signal.
F4 PENDING ACTIVATION	When a DPE is requested to initiate activation it transmits INFO 1 and waits for a response from the PSN.
F5 UNSYN-CHRONIZED	At the first receipt of any signal from the PSN, the DPE ceases to transmit INFO 1 and tries to identify signal INFO 2 or INFO 4.
F6 SYNCHRO-NIZED	When the DPE receives the synchronization signal from the PSN (INFO 2), it responds with INFO 3, indicating that it is in the SYNCHRONIZED state, and waits for normal frames from the PSN (INFO 4).
F7 ACTIVATED	This is the normal active state with the protocol activated in both directions. Both the PSN and the DPE are transmitting frames.
F8 LOST FRAMING	This is the condition when the DPE has lost frame alignment (see 8.3.1) and is awaiting resynchronization by receipt of INFO 2 or INFO 4 or deactivation by receipt of INFO 0.

8.2.1.3 PSN States

The PSN states shall be as follows:

G1 DEACTIVE	The PT is in the idle state, i.e. it is not transmitting.
G2 PENDING ACTIVATION	When a PT is requested to initiate activation it transmits INFO 2 and waits for a response from the DPE (INFO 3).
G3 ACTIVE	The normal active state where the PSN is transmitting INFO 4 to the DPE. The DPE to PSN direction may or may no longer be active, i.e. the PSN may deactivate or maintain the ACTIVATED state if the DPE stops transmitting. (The choice to deactivate is completely up to the PSN).

G4	PENDING DEACTIVATION	When the PSN wishes to deactivate it may wait for a timer (T2) to expire before returning to the DEACTIVE state.

8.2.1.4 Activate Primitives

The following primitives shall be used in the activate procedures:

PH-AR MPH-AR	ACTIVATE REQUEST	These primitives are used to request that the Physical Layer be activated.
PH-AI MPH-AI	ACTIVATE INDICATION	These primitives are used by the Physical Layer to indicate that it has been activated.

8.2.1.5 Deactivate Primitives

The following primitives shall be used in the deactivate procedures:

MPH-DR	DEACTIVATE REQUEST	This primitive is used by the Management Entity to request that the Physical Layer be deactivated.
PH-DI MPH-DI	PH-DEACTIVATE INDICATION	These primitives are used by the Physical Layer to indicate that it has been deactivated.

8.2.1.6 Error and Recovery Primitives

The following primitives shall be used between the Physical Layer and the Management Entity:

MPH-EI1	MPH-ERROR INDICATION 1	MPH-EI1 indicates an error report. The message unit contains the type of the error. This can be: receiving INFO 2 instead of INFO 4; loss of framing.
MPH-EI2	MPH-ERROR INDICATION 2	MPH-EI2 reports that no error condition now exists.
MPH-EI3	MPH-ERROR INDICATION 3	MPH-EI3 indicates that the E-bit received was not equal to the corresponding D-bit. Optional parameters may convey additional information, see 9.4.

8.2.1.7 Connection/Disconnection Primitives

The following primitives shall be used between the Physical Layer and the Management Entity:

MPH-II	MPH-Information INDICATION (c)	MPH-II (c) indicates that the Physical Layer is in the "connected" status.

(d) MPH-II (d) indicates that the Physical Layer is in the "disconnected" status.

8.2.1.8 Primitive Sequences

The primitives defined in 8.2.1.4 to 8.2.1.6 specify, conceptually, the service provided by the Physical Layer to the Data Link Layer and to the Physical Layer Management entity. The constraints on the sequence in which the primitives may occur are specified in Figure 8 and 9. The diagrams do not represent states which must exist for the Physical Layer entity. However, they do illustrate the condition that the Data Link Layer and the Management entities perceive the Physical Layer to be in as a result of the primitives transferred between the entities. Furthermore, the Figures do not represent an interface and are used for modelling purposes only.

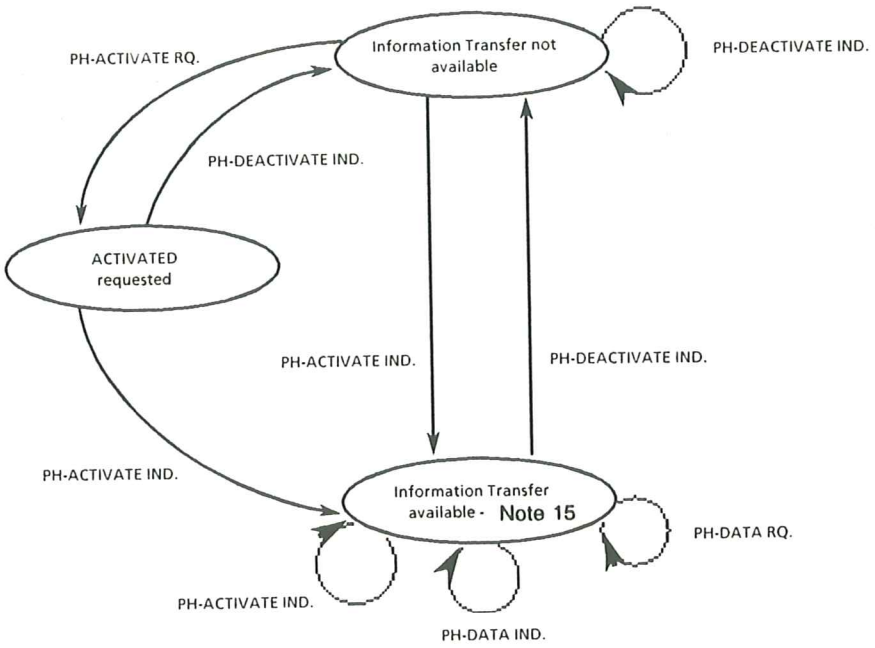


Figure 8 - Primitive Interchange between the Physical Layer and the Data Link Layer

Note 15

The Data Link Layer will not be aware if the information transfer capability is temporarily interrupted.

8.2.2 Activation/Deactivation Procedure at the Terminal Side

When a locally powered DPE is able to detect power source 1, it shall transmit INFO 0, when it is first connected and senses power source 1, or upon the loss of frame alignment, see 8.3.

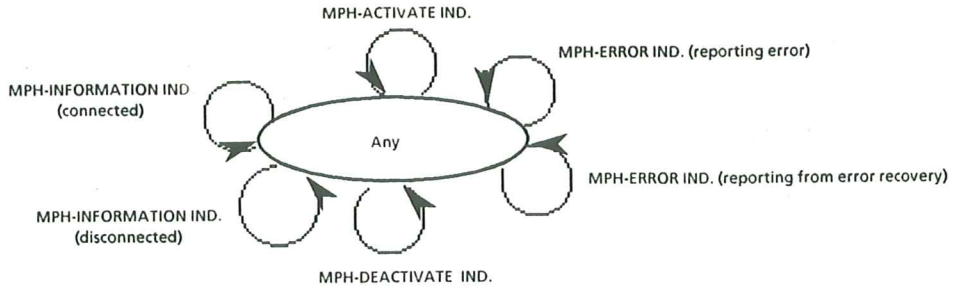


Figure 9 - Primitive Interchange between the Physical Layer and the Management Entity (DPE Side)

Note 16

The use of MPH-ACTIVATE-REQ for maintenance purposes is for future standardization.

When the DPE has achieved frame alignment, it shall transmit INFO 3. The satisfactory transmission of operational data cannot be assured prior to the receipt of INFO 4. Procedures are shown in Table 3.

A DPE which determines that it is connected to a PT not providing power source 1 shall default to the procedures described in Table 4.

STATE NAME	INACTIVE		SENSING	DEACTI-VATED	AVAITING SIGNAL	IDENTI-FYING INPUT	SYNCHRO-NIZED	ACTI-VATED	LOST FRAMING
	Power off	Power on							
State Number	F1.0	F1.1	F2	F3	F4	F5	F6	F7	F8
Info sent	INFO 0	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Loss of power Note 18	/	F1.0	F1.0	MPH-EII(d) MPH-DI, PN-DI; F1.0	MPH-EII(d) MPH-DI, PN-DI; F1.0	MPH-EII(d) MPH-DI, PN-DI; F1.0	MPH-EII(d) MPH-DI, PN-DI; F1.0	MPH-EII(d) MPH-DI, PN-DI; F1.0	PH-EII(d) MPH-DI, PN-DI; F1.0
App. of power Note 18	F1.1	/	/	/	/	/	/	/	/
Detect Power S	/	MPH-EI2 GI2	/	/	/	/	/	/	/
Disapp. Power S	/	/	F1.1	MPH-EII(d) MPH-DI, PN-DI; F1.1	MPH-EII(d) MPH-DI, PN-DI; F1.1	MPH-EII(d) MPH-DI, PN-DI; F1.1	MPH-EII(d) MPH-DI, PN-DI; F1.1	MPH-EII(d) MPH-DI, PN-DI; F1.1	PH-EII(d) MPH-DI, PN-DI; F1.1
(M)PH-Activate Request	/	|	|	ST. T3 F4 Note 19	|	|	–	(M)PH-AI	–
Expiry T3	/	/	–	–	(M)PH-DI; PN-DI; F3	(M)PH-DI; PN-DI; F3	(M)PH-DI; PN-DI; F3	–	–
Receiving INFO 0	/	/	MPH-II(c); F3	–	–	–	MPH-DI; PH-DI; F3	MPH-DI; PH-DI; F3	MPH-DI; PH-DI; MPH-EI2 F3
Receiving any signal Note 17	/	/	–	–	F5	–	/	/	–
Receiving INFO 2	/	/	MPH-II(c); F6	F6	/	F6	–	MPH-EI1; F6	MPH-EI2; F6
Receiving INFO 4	/	/	MPH-II(c); PH-AI; MPH-AI; F7	PH-AI; MPH-AI; F7	/	PH-AI; MPH-AI; F7	PH-AI; MPH-AI; MPH-EI2; F7	–	PH-AI; MPH-AI; MPH-EI2; F7
Lost Framing	/	/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	–

Legend: | Impossible due to the definition of the Physical Layer service
– No Change
/ Impossible Situation
P;Fn means: "Issue primitive P and then go to state Fn"
Primitives: The indexes "(c)" and "(d)" indicate "connected" and "disconnected", respectively.

Table 3 - Activation/Deactivation for locally powered DPEs, able to detect Power Source 1

(Use confined to PTs which provide power source 1)

Note 17

This event reflects the case where some signal is received and the DPE has not (yet) determined whether it is INFO 2 or INFO 4.

Note 18

The term "power" may designate full operational or backup power. Backup power is defined to provide enough energy to hold the TEI value in memory and to maintain the capability of receiving and transmitting the Data Link Layer frames associated with the TEI assignment procedure.

Note 19

Timer T3 may be implemented in the Physical Layer or elsewhere.

A functional SDL description of the procedure is presented in 8.2.5.

Locally powered DPEs shall, when power is removed, initiate the transmission of INFO 0 before frame alignment is lost.

8.2.3 Activation/Deactivation Procedure at the PSN Side

This procedure is beyond the scope of this Standard. For the provision of background information, however, it is shown in Table 4 in the form of a finite state matrix. A functional SDL description of the procedure is presented in 8.2.4.

STATE NAME	INACTIVE	SENSING	DEACTI-VATED	AVAITING SIGNAL	IDENTI-FYING INPUT	SYNCHRO-NIZED	ACTI-VATED	LOST FRAMING
State Number	F1.0	F2	F3	F4	F5	F6	F7	F8
Info sent	INFO 0	INFO 0	INFO 0	INFO 1	INFO 0	INFO 3	INFO 3	INFO 0
Loss of power Note 21	/	F1	MPH-II(d) F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1	MPH-II(d) MPH-DI, PH-DI; F1
App. of power Note 21	F2	/	/	/	/	/	/	/
Detect Pwr S. 1	/	/	/	/	/	/	/	/
Disapp. Pwr S. 1	/	/	/	/	/	/	/	
(M)PH-Activate Request	/	|	Start T3 F4 Note 22	|	|	–	(M)PH-AI	–
Expiry T3	/	/	–	MPH-DI; PN-DI; F3	MPH-DI; PN-DI; F3	MPH-DI; PN-DI; F3	–	–
Receiving INFO 0	/	MPH-II(c); F3	–	–	–	MPH-DI; PH-DI; F3	MPH-DI; PH-DI; F3	MPH-DI; PH-DI; MPH-EI2 F3
Receiving any signal Note 20	/	–	–	F5	–	/	/	–
Receiving INFO 2	/	MPH-II(c); F6	F6	/	F6	–	MPH-EI1; F6	MPH-EI2; F6
Receiving INFO 4	/	MPH-II(c); PH-AI; MPH-AI; F7	PH-AI; MPH-AI; F7	/	PH-AI; MPH-AI; F7	PH-AI; M;PH-AI; MPH-EI2; F7	–	PH-AI; M;PH-AI; MPH-EI2; F7
Lost Framing	/	/	/	/	/	MPH-EI1; F8	MPH-EI1; F8	–

Legend: | Impossible due to the definition of the Physical Layer service
– No Change
/ Impossible Situation
P;Fn means: "Issue primitive P and then go to state Fn"
Primitives: The indexes "(c)" and "(d)" indicate "connected" and "disconnected", respectively.

Table 4 - Activation/Deactivation for DPEs locally powered, not able to detect Power Source 1

Note 20

This event reflects the case where some signal is received and the DPE has not (yet) determined whether it is INFO 2 or INFO 4.

Note 21

The term "power" may designate full operational or backup power. Backup power is defined to provide enough energy to hold the TEI value in memory and to maintain the capability of receiving and transmitting the Data Link Layer frames associated with the TEI assignment procedure.

Note 22

Timer T3 may be implemented in the Physical Layer or elsewhere.

STATE NAME	DEACTIVE *(Note 4)*	PENDING ACTIVATION	ACTIVE	PENDING DEACTIVATION *(Note 4)*
State Number	G1	G2	G3	G4
Info sent	INFO 0	INFO 2	INFO 4	INFO 0
(M)PH-Activate Request	set T1 Note 23 G2	/	(M)PH-AI	set T1 Note 23 G2
(M)PH-Deactivate Request	MPH-DI	set T2 Note 24 (M)PH-DI; G4	set T2 Note 24 (M)PH-DI; G4	–
Expiry of Timer T1 Note 23	–	set T2 Note 24 (M)PH-DI; G4	/	–
Expiry of Timer T2 Note 24	–	–	–	G1
Receiving INFO 0	–	–	(M)PH-DI; (M)PH-EI; G2	G1
Receiving INFO 1	set T1 Note 23 G2	–	/	–
Receiving INFO 3	/	set T1 Note 23 (M)PH-AI; G3 Note 25	–	–
Loss of framing	/	/	(M)PH-DI; (M)PH-EI; G2	–

Legend: – No Change
/ Impossible Situation
P;Gn means: "Issue primitive P and then go to state Gn"

Table 5 - Activation/Deactivation of the Physical Layer at the PSN Side

Note 23

Timer T1 is a supervisory timer which has to take into account the overall time to activate.

Note 24

Timer T2 prevents unintentional reactivation. Its value is between 25 ms and 100 ms. This implies that a DPE has to recognize INFO 0 and to react on it within 25 ms. If the PSN is able to unambiguously recognize INFO 1, then the value of timer T2 may be 0.

Note 25

As an option, the primitive and INFO 4 may be send only 100 ms, after INFO 3 has been received.

Note 26

Some PTs may never deactivate. In this case, they never enter states G1 nor G4, and timers T1 and T2 do not exist.

8.2.4 SDL Presentation of the Activation/Deactivation Procedure

Figures 10 to 19 show the interworking between the DPE and (as far as applicable and necessary for understanding) the PSN side of the Physical Layer Activation/Deactivation protocol. The protocol is partitioned as follows:

Transition from the POWER-OFF to the DEACTIVATED state
The DPE is forced to re-enter the SYNCHRONIZED state
Activation initiated by the DPE
Activation Failure at the DPE side
Status Verification
The DPE has lost Framing
The DPE has lost Power
The PSN releases the Physical Layer Connection
Activation initiated by the PSN

The activation/deactivation signals are continuous signals. An (external) output symbol indicates that the transmission of such continuous signal is to be started. The transmission of this signal ends when it is replaced by another signal to be sent in the same direction. An (external) input symbol indicates that an incoming signal has arrived.

The SDL symboling used assumes that the DPE is on the left and the PSN is on the right hand side of a functional interworking model as depicted in Figure 10.

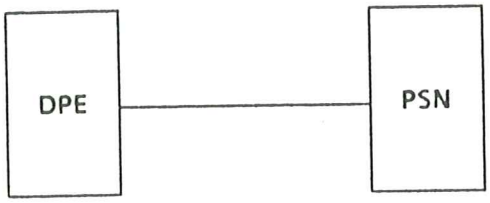
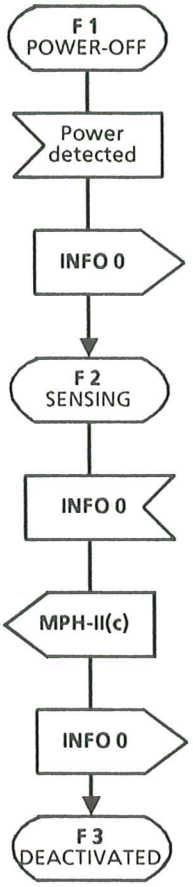
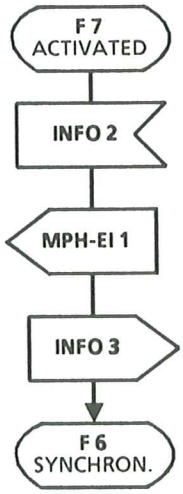


Figure 10 - Functional Interworking Model



There is no corresponding sequence at the PSN side of the S_0 interface.

Figure 11 - Transition from the INACTIVE to the DEACTIVATED State



The corresponding sequence at the PSN side of the S_0 interface is out of the scope of this Standard.

Figure 12 - The DPE is forced to re-enter the SYNCHRONIZED State

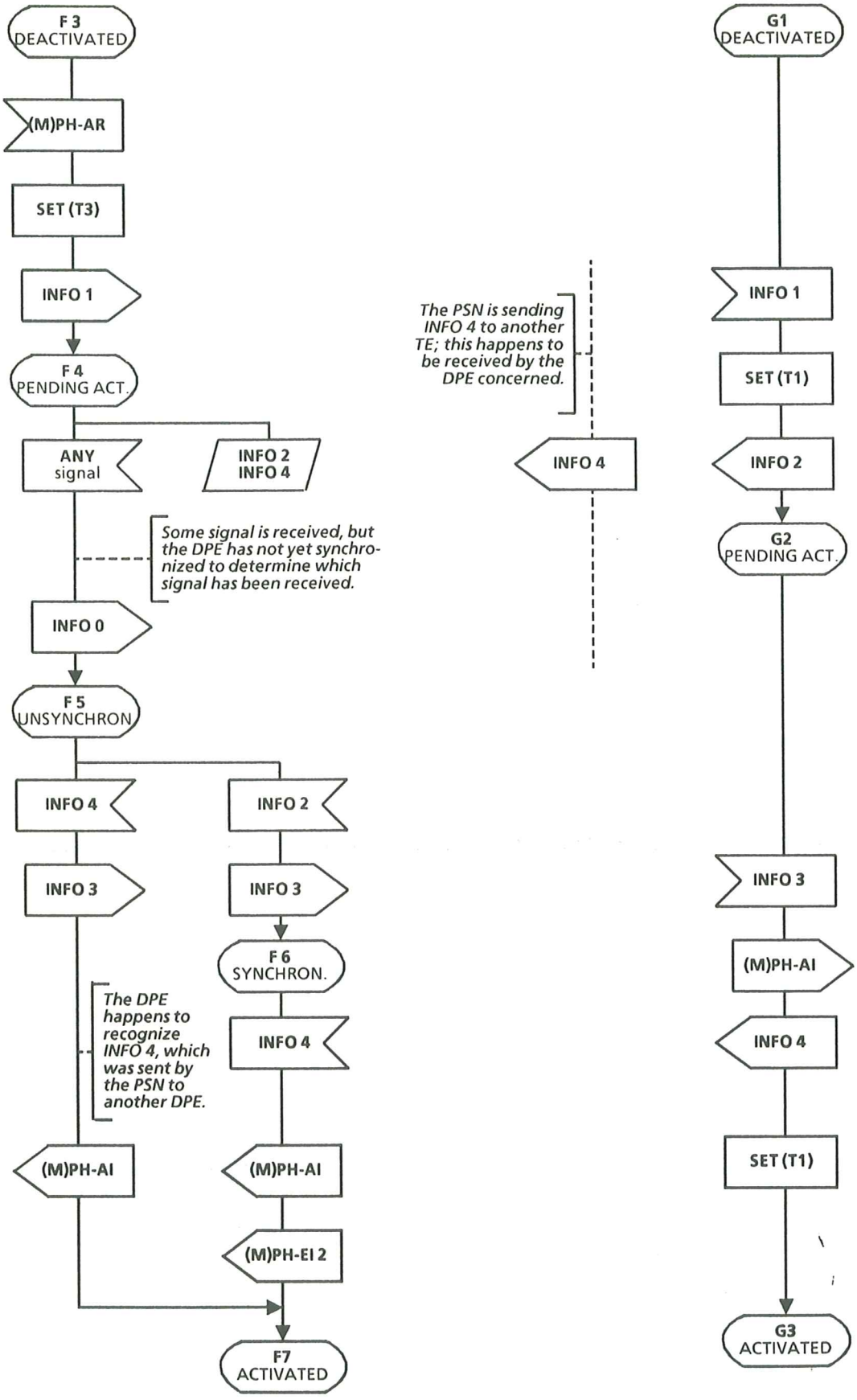


Figure 13 - Activation initiated by the DPE

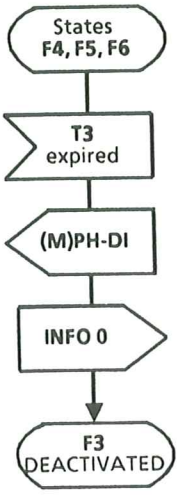


Figure 14 - Activation Failure at the DPE Side

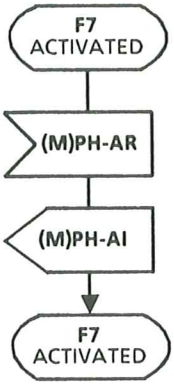


Figure 15 - Status Verification

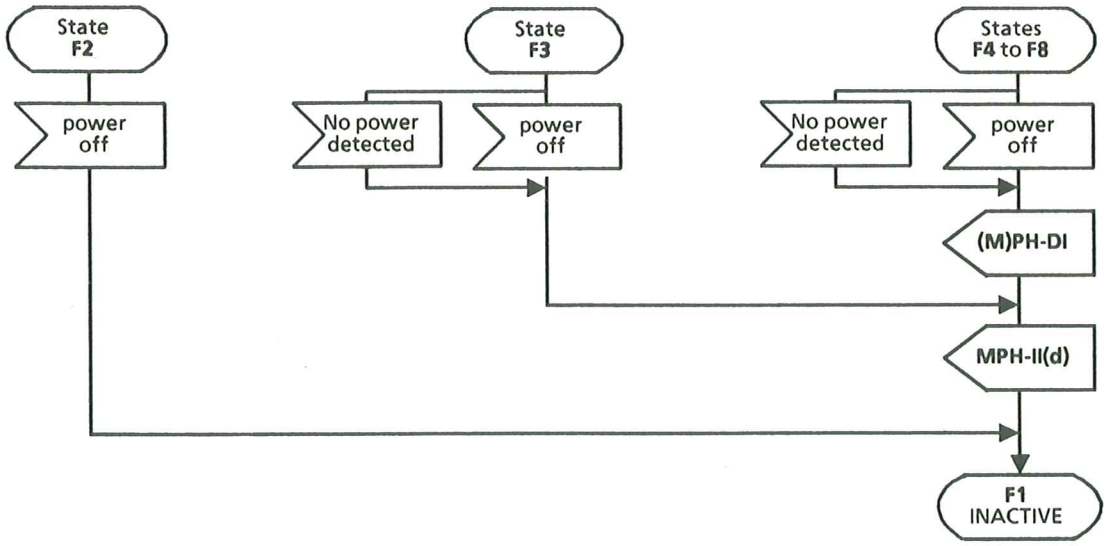


Figure 16 - The DPE has lost Power or does not detect Power at the Interface

Note 27

Only relevant, if the DPE monitors power at the S_0 interface.

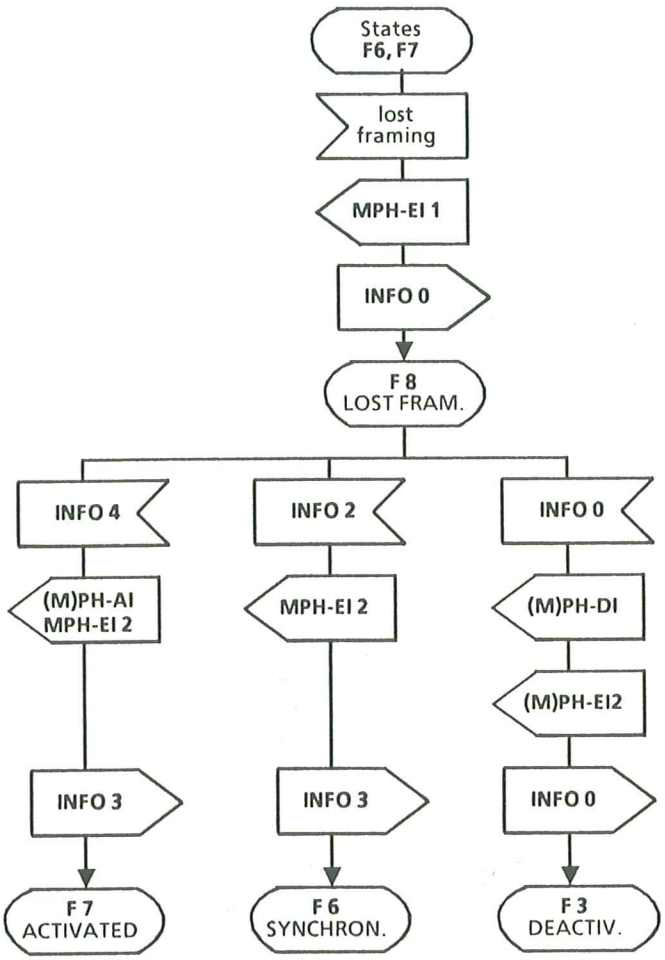


Figure 17 - The DPE has lost Framing

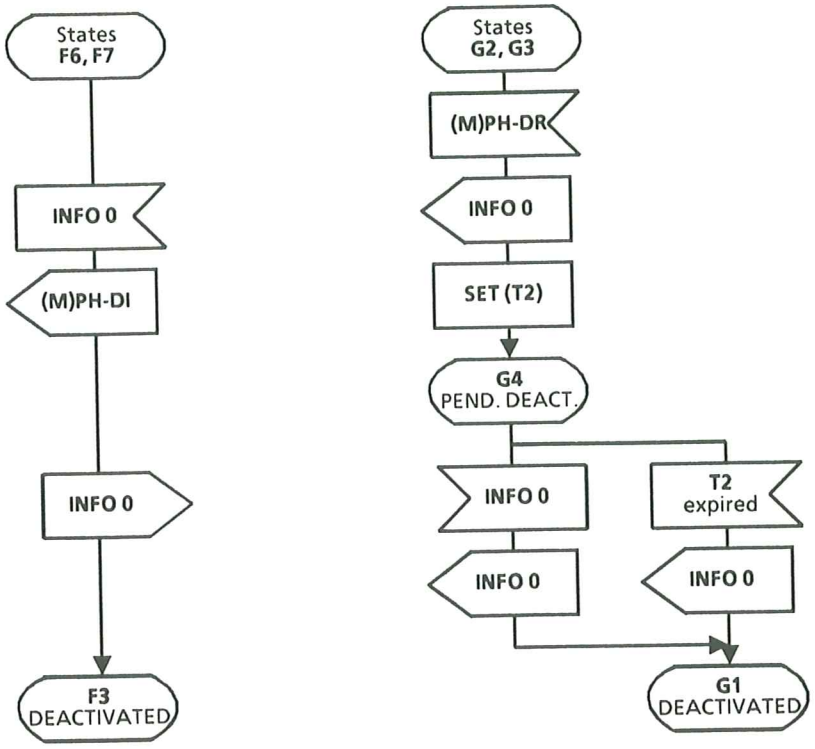


Figure 18 - The PSN Releases the Physical Layer Connection

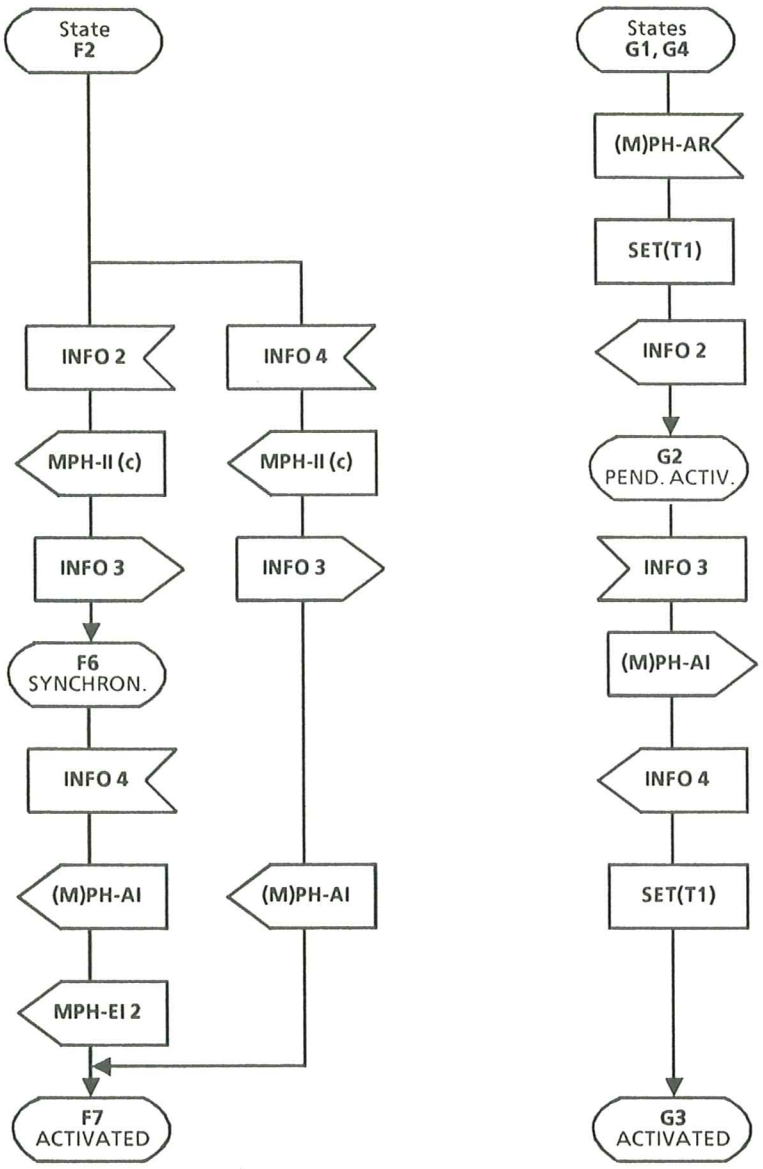


Figure 19 - Activation initiated by the PSN

8.2.5 Timing Values

8.2.5.1 Timers

The expiry of timers is used to select an alternative sequence in order to continue and conclude the procedure in an orderly fashion even when an expected reaction fails.

Three timers shall be used in the Physical Layer protocol:

PSN side

Timer T1 supervises whether or not the Physical Layer can be activated by the PSN. The specification of its value is outside the scope of this Standard.
Timer T2 gives the TEs sufficient time to recognize INFO 0 and to enter the DEACTIVATED state. According to CCITT Rec. I.430, its value is specified as 25 ms to 100 ms.

DPE side

Timer T3 gives the PSN sufficient time to recognize INFO 1 and to respond by transmitting INFO 2. The value of T3 shall be 3 s.
If the PSN fails to respond before T3 expires, a reattempt may be initiated by higher layers or the Management Entity.

8.2.5.2 Reaction Times of the DPE

In the SYNCHRONIZED state the DPE shall recognize the receipt of INFO 4 within two frames (in the absence of errors).

The DPE shall send INFO 3 within 100 ms of receipt of INFO 2 or INFO 4.

In accordance with CCITT Rec. I.430, the DPE shall react on INFO 0 within 25 ms.

8.3 Frame Alignment Procedures

The first bit of each frame shall be the framing bit F; it shall be a ZERO.

The frame alignment procedures makes use of the fact that the framing bit is represented by a pulse having the same polarity as the preceding pulse which is a violation of the alternate mark inversion (AMI) scheme; this intentional violation is used for reframing.

To guarantee secure framing the auxiliary framing bit pair F_A and N in the direction PT to DPE or the auxiliary framing bit F_A with the associated balancing bit L in the direction DPE to PT are introduced. For the direction PT to DPE, this ensures that there is always an AMI violation at 14-bits or less (the 14-bit criterion) from the framing bit F, due to F_A or N being a ZERO. For the direction DPE to PT, it ensures that there is always an AMI violation at 13-bits or less (the 13-bit criterion), due to F_A being always ZERO. The framing procedures do not depend on the polarity of the framing bit F and thus are not sensitive to wiring polarity.

The coding rule for the auxiliary framing bit pair F_A and N in the direction PT to DPE is such that N is the binary opposite of F_A, i.e.:

$$N = \overline{F_A}$$

The F_A and L bit in the direction DPE to PT are always coded such that the binary values of F_A and L are equal.

8.3.1 Frame Alignment Procedure in the Direction PT to DPE

Frame alignment on initial activation of the DPE shall comply with the timing value defined in 8.2.6.2.

8.3.1.1 Loss of frame alignment shall be assumed when a time period equivalent to two 48-bit frames has elapsed without having detected valid pairs of AMI violations, obeying the 14-bit criterion as described above. The DPE shall cease transmission immediately.

8.3.1.2 Frame realignment shall be assumed to occur when 3 consecutive pairs of line AMI violations, obeying the 14-bit criterion, have been detected.

8.3.2 Frame Alignment in the Direction DPE to PT

The 13-bit criterion shall apply.

8.3.2.1 The PT may assume loss of frame alignment if a time period equivalent to two 48-bit frames has elapsed since detecting consecutive violations according to the 13-bit criterion. On detection of loss of framing, the PT shall either continue transmitting towards the DPE (i.e. remain in the ACTIVATED state) or initiate deactivation by transmitting INFO 0 (i.e. take the PENDING DEACTIVATION state).

8.3.2.2 The PT may assume that frame alignment has been regained when 3 consecutive pairs of AMI violations, obeying the 13-bit criterion, have been detected.

8.4 Idle Channel Code on B-Channels

A DPE shall send ONEs in any B-channel which is not assigned to it. This is the responsibility of higher layers.

8.5 Multiframing

An optional multiframe provides extra transmission capacity within the Physical Layer in the DPE-to-PT direction by the use of an additional channel called Q-channel. The Q-channel is unidirectional, i.e. there is no Q-channel in the PT-to-DPE direction. DPEs not using the Q-channel shall set each Q-bit to binary ONE.

Although the use of the Q-channel is the same in point-to-point and in point-to multipoint configurations, no collision detection mechanism is provided within the scope of this Standard.

8.5.1 Q-Bit Identification

The Q-bits (DPE-to-PT direction) are defined to be at the F_A-bit positions of every fifth frame. The Q-bit positions in the DPE-to-PT direction are identified by inversions of the F_A/N-bit pair (F_A = ONE, N = ZERO) in the opposite direction. The provision of the capability in the PT depends on the implementation of the specific PSN. The provision for identification of the Q-bit positions in the direction PT-to-TE permits all DPEs to synchronize their trans-

mission over the Q-channel and thus to avoid interference of F_A-bits of one TE with the Q-bits of a second TE in passive bus configurations.

8.5.2 Multiframe Identification

A multiframe which provides for structuring the Q-bits in groups of four (Q1 to Q4) shall be established by setting the M-bit (position 26 of the PT-to-DPE frame) to ONE in every twentieth frame. This structure provides a single channel for four-bit characters in the direction DPE to PT.

8.5.3 Q-Bit Position Identification Algorithm

The Q-bit position identification algorithm is illustrated in Table 6.

Frame Number	PT-to-DPE F_A-Bit Position	DPE-to-PT F_A-Bit Position	PT-to-DPE M-Bit
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
3	ZERO	ZERO	ZERO
4	ZERO	ZERO	ZERO
5	ZERO	ZERO	ZERO
6	ONE	Q2	ZERO
7	ZERO	ZERO	ZERO
8	ZERO	ZERO	ZERO
9	ZERO	ZERO	ZERO
10	ZERO	ZERO	ZERO
11	ONE	Q3	ZERO
12	ZERO	ZERO	ZERO
13	ZERO	ZERO	ZERO
14	ZERO	ZERO	ZERO
15	ZERO	ZERO	ZERO
16	ONE	Q4	ZERO
17	ZERO	ZERO	ZERO
18	ZERO	ZERO	ZERO
19	ZERO	ZERO	ZERO
20	ZERO	ZERO	ZERO
1	ONE	Q1	ONE
2	ZERO	ZERO	ZERO
etc			

Table 6 - Q-Bit Position Identification and Multiframe Structure

Note 28

DPEs not using the Q-bits shall set them to ONE.

Note 29

Where multiframe identification is not provided with a ONE in an appropriate M-bit, but where Q-bit positions are identified, Q-bits 1 to 4 are not distinguished.

Two examples of how such an identification algorithm can be realized are:

- The DPE Q-bit identification algorithm may be simply the transmission of a Q-bit in each frame in which a ONE is received in the F_A-bit position of the PT-to-DPE frame (i.e. by echoing the received F_A-bits).
- Alternatively, to minimize the Q-bit transmission errors that could result from errors in the F_A-bits of the PT-to-DPE frames, a DPE may synchronize a frame counter to the Q-bit rate and transmit Q-bits in every fifth frame, i.e. in frames in which F_A-bits should be present. Q-bits would be transmitted only after counter synchronization to the ONEs in the F_A-bit position of the PT-to-DPE frames is achieved (and only if such bits are received). When the counter is not synchronized (synchronization not achieved or lost), a DPE which uses such an algorithm shall transmit ZEROs over the Q-channel. The algorithm used by a DPE to determine when synchronization is defined to be achieved, or the algorithm used to determine when it is defined to be lost, is outside the scope of this Standard.

8.5.4 Multiframe Identification by the DPE

The first frame of the multiframe shall be identified by the M-bit equal to a ONE. DPEs that are not intended to use nor to provide for the use of the Q-channel are not required to identify the multiframe. DPEs that are intended to use or to provide the use of the Q-channel shall use the M-bit equal to a ONE to identify the beginning of a multiframe.

The algorithm employed by a DPE to determine when synchronization or loss of synchronization of the multiframe is achieved, is beyond the scope of this Standard.

The transmission of multiframes by the PT depends on the actual PSN implementation.

9. PROVISIONS FOR PHYSICAL LAYER MAINTENANCE

The Physical Layer shall provide the following maintenance facilities:

9.1 Test Loopback

Two test loopbacks, Loopback A4 and Loopback B4, can be activated, see Figure 20.

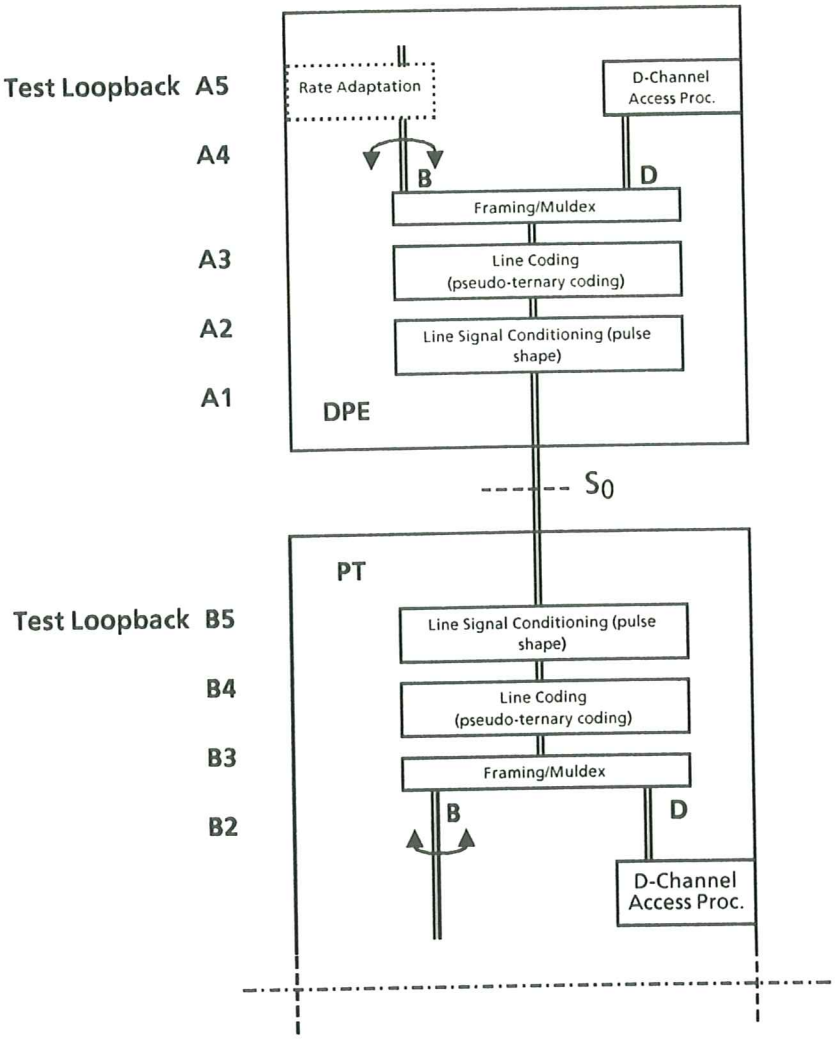


Figure 20 - DPE and PSN (PT) Test Loopbacks

Loopback A4 shall provide a loopback of both B-channels independently towards the PSN. The loopback shall preserve octet integrity. It shall reflect any bit pattern received on a B-channel.

The earliest point in time when the PT will receive the looped information shall correspond to a delay of 2 bits (see 7.4).

Loopback B4 whether or not Loopback B4 is provided depends on the implementation of the specific PSN. When provided, it shall loopback both B-channels independently towards the DPE. The loopback shall preserve octet integrity. The DPE will see a delay of at least 22 bits of any bit pattern applied to the S_0 interface.

9.2 Management Entity Primitives

The test loopback shall be activated and deactivated by the Management Entity by means of the primitives:

MPH-LAR	MPH-LOOP ACTIVATION REQUEST	The parameters shall indicate the type of the loopback and the channel(s), where appropriate.
MPH-LDR	MPH-LOOP DEACTIVATION REQUEST	The parameters shall indicate the type of the loopback and the channel(s), where appropriate.

The activated or deactivated state of the loop(s) shall be indicated to the Management Entity by means of the primitives.

MPH-LAI	MPH-LOOP ACTIVATION INDICATION	The parameters shall indicate the type of the loopback and the channel(s), where appropriate.
MPH-LDI	MPH-LOOP DEACTIVATION INDICATION	The parameters shall indicate the type of the loopback and the channel(s), where appropriate.

9.3 Test Bit Stream

9.3.1 Continuous ZEROs

The DPE shall provide the facility to transmit a continuous bit stream consisting of ZEROs. This facility shall not be activated or deactivated via the S_0 interface. Optionally the PSN may also provide the facility to transmit a continuous bit stream consisting of ZEROs. For the use of the continuous ZEROs bit stream see 10.5.6.2.

9.3.2 Isolated ZEROs

In the SYNCHRONIZED state the DPE shall provide the facility to transmit a bit pattern coded 11110111 on both B-channels. The isolated ZEROs bit stream shall be used to measure the pulse shapes of the output signal, see 10.5.3.

9.4 D-Echo-Bit

When the E-bit differs from the corresponding D-bit, the MPH-EI 3 primitive may be sent to the Management Entity. Distinction between bit errors ans access collisions (see 8.1.5) by the Management Entity is possible if additional information is conveyed by optional parameters of the primitive (i.e. the bit position of the error and the contents of the associated PH-DATA-REQUEST).

10. ELECTRICAL CHARACTERISTICS

From the view point of their electrical characteristics, connection cords and plugs are considered to be part of the DPE.

10.1 Bit Rate

The nominal bit rate at the S_0 interface shall be 192 kbit/s in both directions of transmission, with a tolerance of not more than ± 100 ppm in the free running mode.

10.2 Jitter and Bit Rate Relationship between DPE Input and Output

10.2.1 Test Configuration

The jitter and phase deviation measurements shall be carried out with four different wave forms at the terminal input, in accordance with the following configurations:

I	Point-to-point configuration with 6 dB attenuation measured between the two termination resistors at 96 kHz (high-capacitance cable);
II	Short passive bus with 8 terminals (including the terminal under test) clustered at the far end from the signal source (high-capacitance cable);
IIIa, IIIb	Short passive bus with the terminal under test adjacent to the signal source, and the other seven terminals clustered at the far end from the signal source (high and low capacitance cable);
IV	Ideal test signal condition, with the source connected directly to the receiver of the terminal under test (i.e. without artificial line).

Examples for wave forms that correspond to the configurations I, II, IIIa and IIIb are given in Figures 21 to 24. Test configurations which can generate these signals are given in Figure 25.

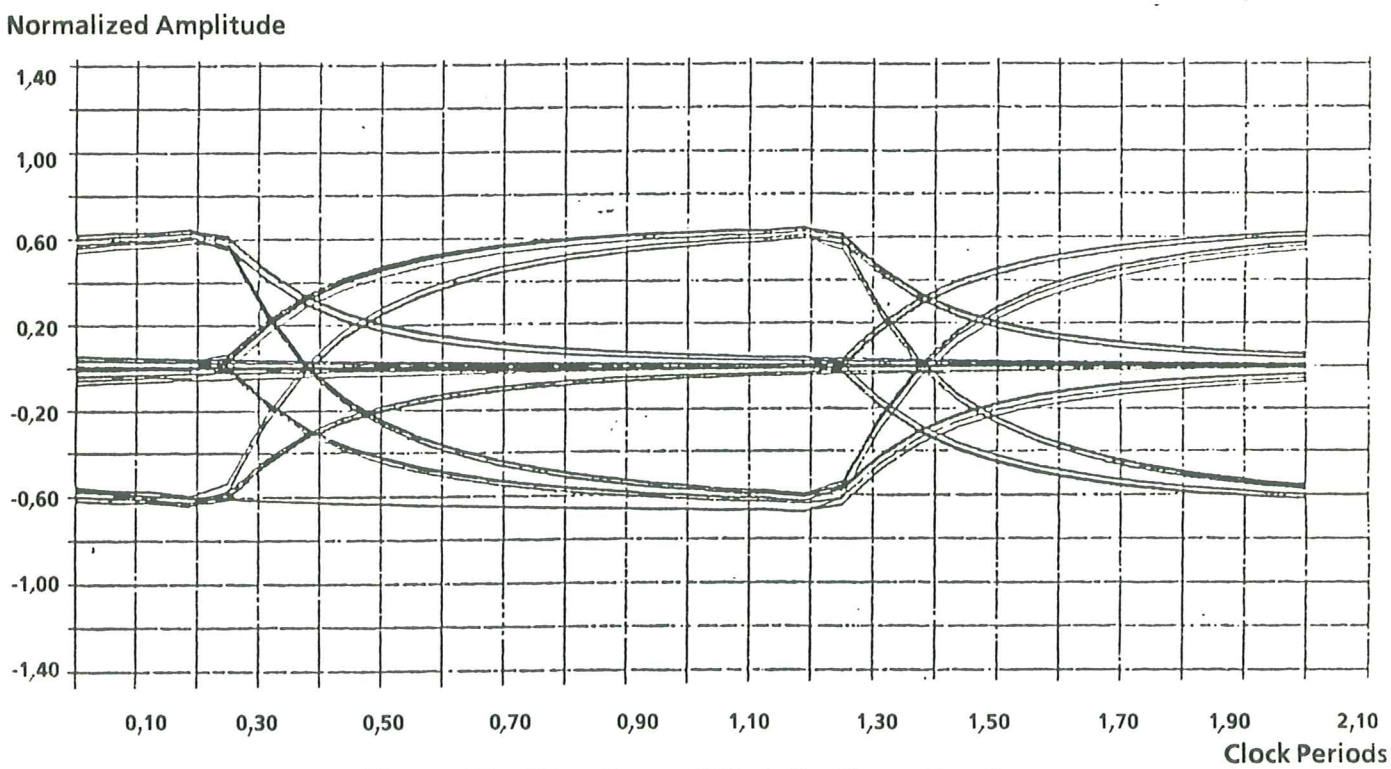


Figure 21 - Waveform of Test Configuration I:
Point-to-point (6 dB)
(C = 120 nF/km)

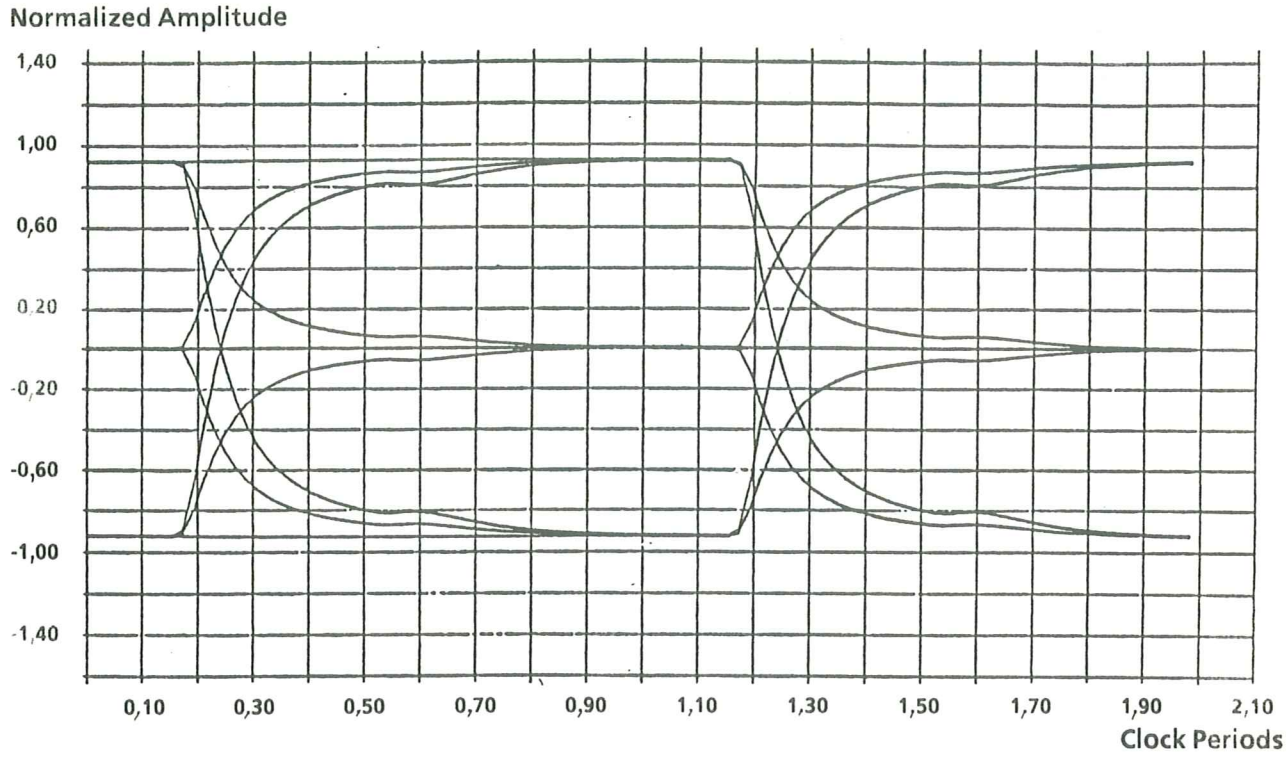


Figure 22 - Waveform of Test Configuration II:
Short Passive Bus with 8 clustered TEs at the far End
(C = 120 nF/km)

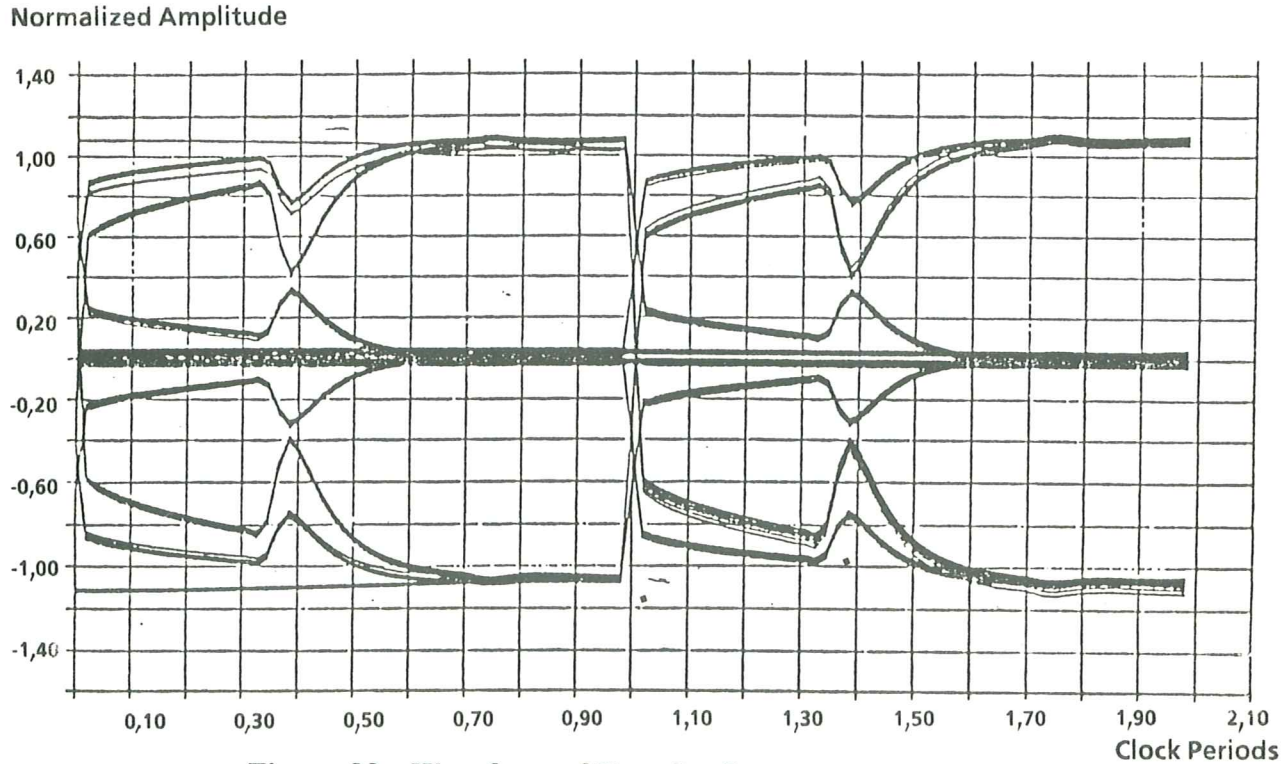


Figure 23 - Waveform of Test Configuration IIIa:
Short Passive Bus with 1 TE near to the PT, and 7 TEs at the far End
(C = 120 nF/km)

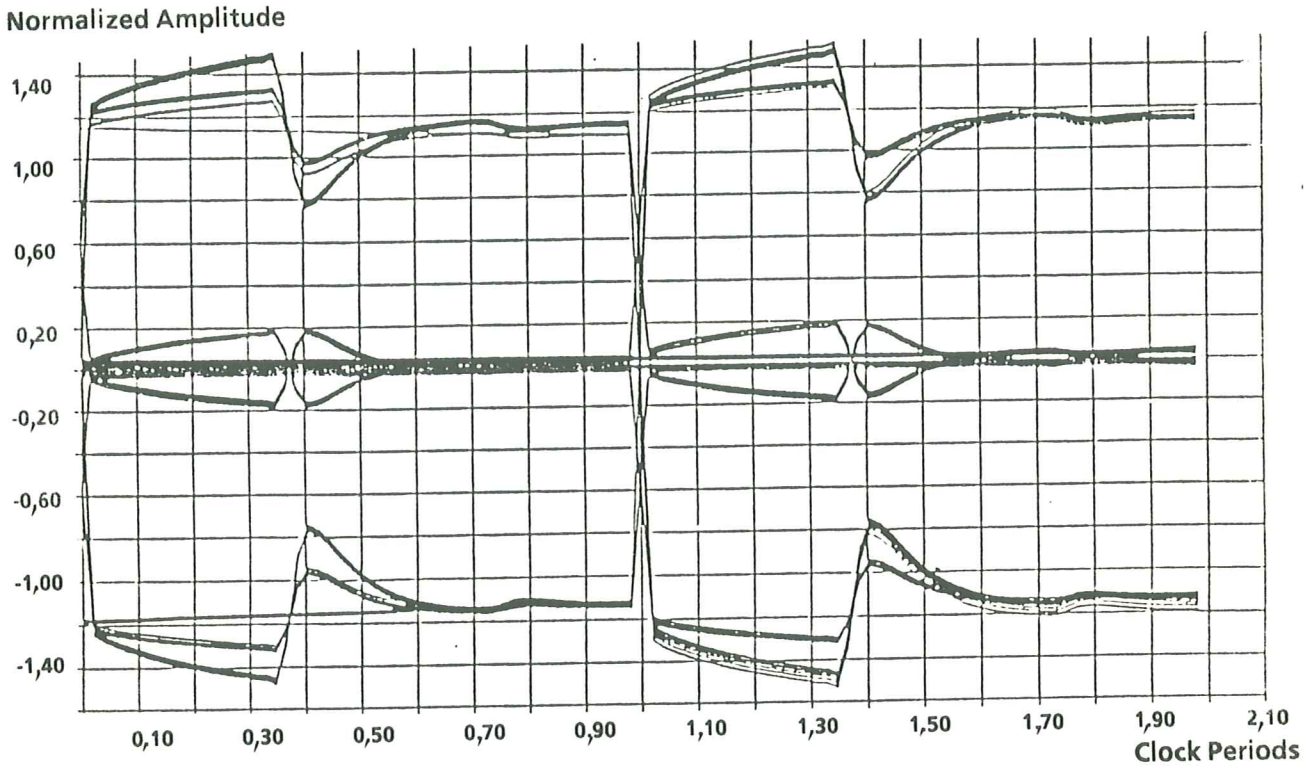
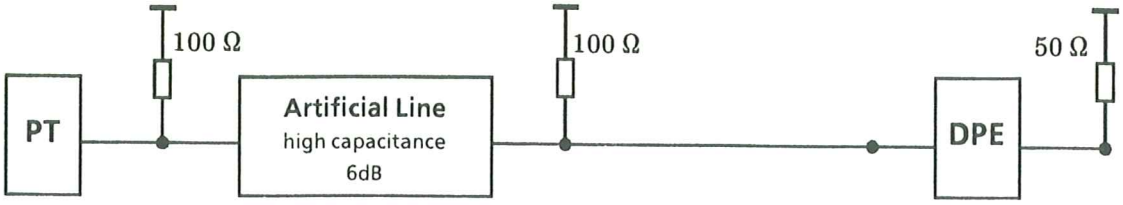
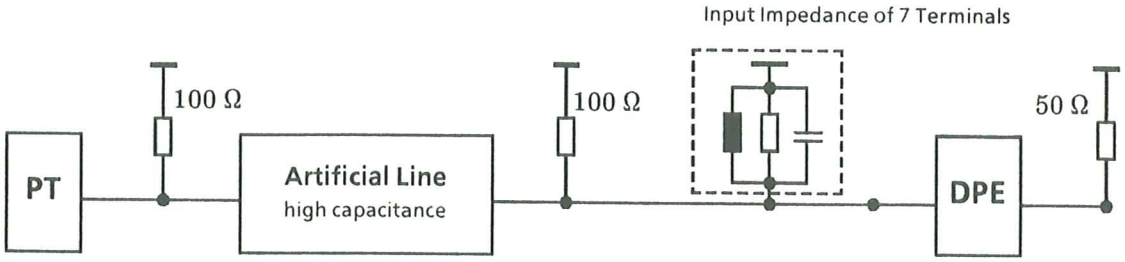


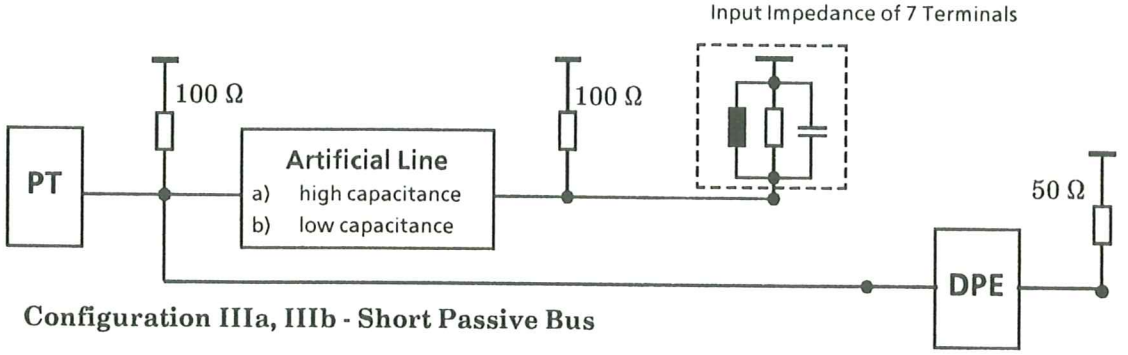
Figure 24 - Waveform of Test Configuration IIIb:
Short Passive Bus with 1 TE near to the PT, and 7 TEs at the far End
(C = 30 nF/km)



Configuration I - Point-to-Point



Configuration II - Short Passive Bus



Configuration IIIa, IIIb - Short Passive Bus

Configuration IV - Ideal Test Signal

Figure 25 - Test Configurations for the Generation of Waveforms

Note 30

The artificial lines are used to derive the waveforms. For test configurations II and III, the cable length corresponds to a signal delay of 1 µs. The parameters for the artificial lines are:

	High capacity cable	*Low capacity cable*
R (96kHz)	*160 Ω/km*	*160 Ω/km*
C (1 khz)	*120 nF/km*	*30 nF/km*
Z0 (96 khz)	*75 Ω*	*150 Ω*
Wire diameter	*0,6 mm*	*0,6 mm*

10.2.2 Timing Extraction Jitter

Timing extraction jitter due to the DPE shall be within the range -7% to +7% of a bit period when the jitter is measured using a high pass filter with a cut-off frequency (3 dB point) of 30 Hz under test conditions described in 10.2.1. The limitation applies with an output data sequence having ZEROs in both B-channels and with input data sequences described in a) to c) following. The limitation applies to the phase of all zero volt crossings of all adjacent ZEROs in the output data sequence.

a) A sequence consisting of continuous frames with all ONEs in D, D-echo and both B-channels;

b) A sequence, repeated continuously for at least 10 seconds, consisting of:

- 40 frames with continuous octets of "10101010" (the first bit to be transmitted is ONE) in both B-channels and continuous ONEs in D and D-echo channels followed by,

- 40 frames with continuous ZEROs in D, D-echo and both B-channels.

c) A sequence consisting of a pseudo random pattern with a length of 2^{19}-1 in D, D-echo and both B-channels. (This pattern may be generated with a shift register with 19 stages with the outputs of the first, second, the fifth and the nineteenth stages added together (modulo 2) and fed back to the input).

10.2.3 Total Phase Deviation

The total phase deviation (including effects of timing extraction jitter in the DPE) between the transitions of signal elements at the output of the DPE relative to the transitions of signal elements associated with the signal applied to the DPE input shall be in the range of - 7% to + 15% of a bit period. This limitation applies to the output signal transitions of each frame with the phase reference defined as the average phase of the crossing of zero volts, which occurs between the framing pulse and its associated balance pulse at the start of the frame and the corresponding crossings at the start of the three preceding frames of the input signal.

For the purposes of demonstrating compliance of a piece of equipment, it is sufficient to use (as the input signal reference) only the crossing of zero volts between the framing pulse and its associated balance pulse of the individual frame. This latter method, requiring a simpler test set, may create additional jitter at frequencies higher than about 1 kHz and is therefore more restrictive.

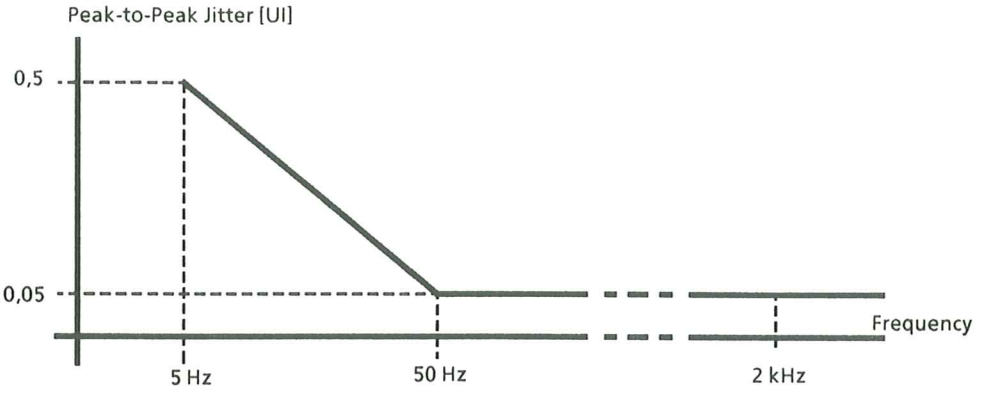
The limitation applies to all test conditions described in 10.2.1 and to the phase of all zero volt crossings of all adjacent ZEROs in the output data sequence (as defined in 10.2.2), with the additional input signal conditions specified in a) to d) following. In addition, a jitter is superimposed as specified in Figure 26, over the range from 5 Hz to 2 kHz. The limitation applies for input bit rates of 192 kbit/s ± 100 ppm.

a) A sequence consisting of continuous frames with all ONEs in D, D-echo and both B-channels;

b) A sequence consisting of continuous frames with the octet "10101010" (the first bit to be transmitted is ONE) in both B-channels and continuous ONEs in D and D-echo channels;

c) A sequence of continuous frames with ZEROs in D, D-echo and both B-channels;

d) A sequence of continuous frames with a pseudo random pattern as described in 10.2.2 point c), in D, D-echo and both B-channels.



Legend: UI = Unit Interval

Figure 26 - Lower Limit of Maximum Tolerable Jitter at DPE Input (log/log-scale)

10.3 PT Jitter Characteristics

The maximum output jitter (peak-to-peak) shall be in accordance with CCITT Rec. I.430.

10.4 Termination of the Line

The line impedance of the in-house cabling shall be in accordance with CCITT Rec. I.430 (approximately 100 Ω; it will be terminated by a terminating resistor forming part of the in-house cabling (see Figure 27)).

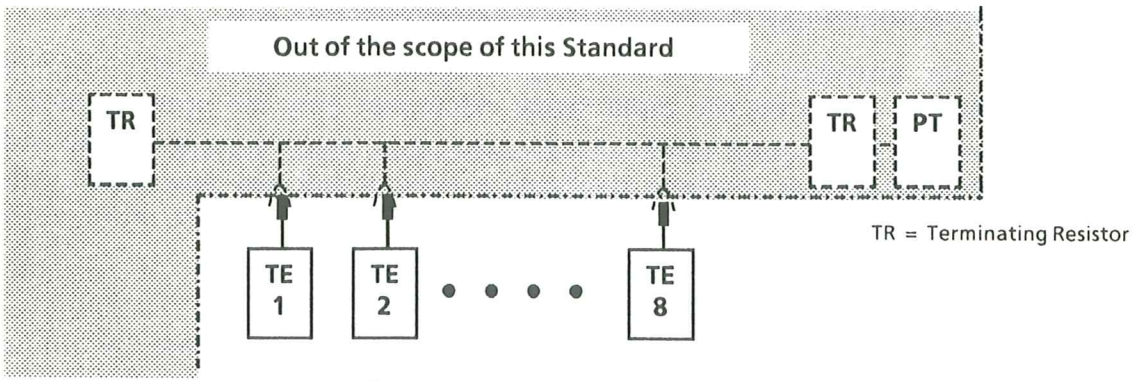


Figure 27 - Termination of the Line

10.5 DPE Output Characteristics

10.5.1 DPE Output Impedance

The following requirements for DPEs shall apply at the interface connector:

When sending ONEs, the following requirements apply:

I The impedance, in the frequency range of 2 kHz to 1 MHz, shall exceed the template in Figure 28. This requirement is applicable with an applied sinusoidal voltage of at least 100 mV_{rms}.

II At a frequency of 96 kHz the peak current resulting from an applied voltage of up to 1,2 V_{peak} shall not exceed 0,6 mA_{peak}.

When sending ZEROs, the output impedance shall be ≥ 20 Ω.

Note 31

The output impedance limit shall apply for two nominal load impedance (resistive) conditions: 50 Ω and 400 Ω. The output impedance for each nominal load shall be defined by determining the peak pulse amplitude for loads equal to the nominal value ± 10%. The peak amplitude shall be defined as the amplitude at the midpoint of a pulse. The limitation applies for pulses of both polarities.

Figure 28 shows the template for the DPE output impedance.

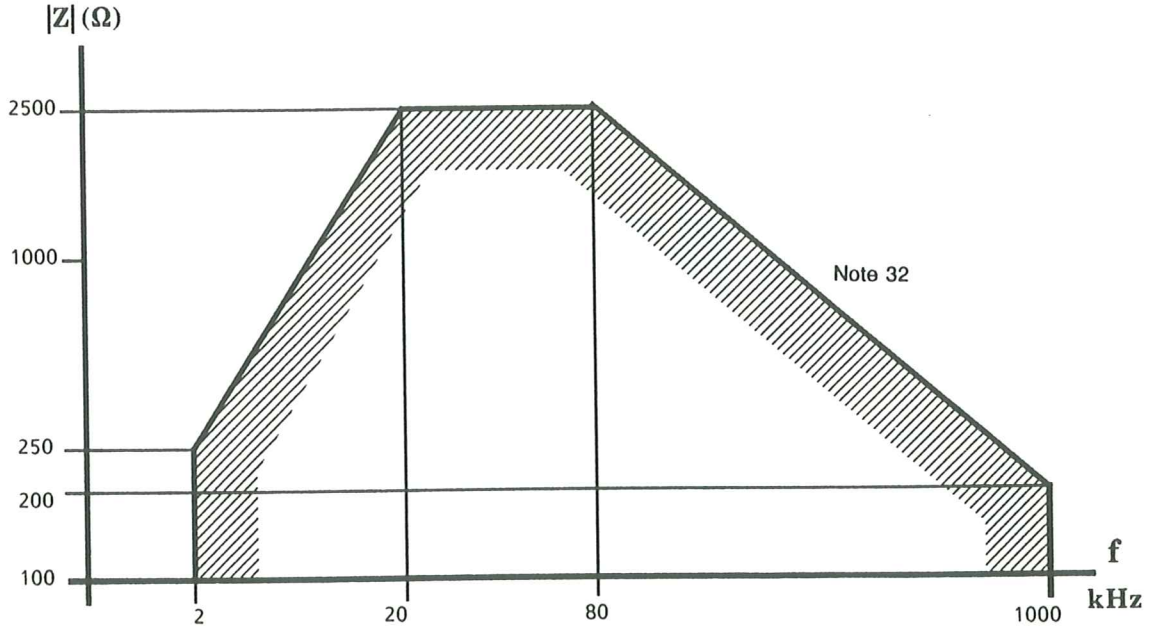


Figure 28 - DPE Impedance Template, including Connection Cord and Plug (log/log scale)

Note 32

The slope corresponds to a capacitance load of 800 pF for the DPE including its connection cord and connectors.

10.5.2 Test Load Impedance

Unless otherwise indicated, the test load impedance shall be 50 Ω.

10.5.3 Pulse Shape and Amplitude (ZERO)

10.5.3.1 Pulse Shape

Except for overshoots, limited as follows, the pulse shape shall be within the mask of Figure 29. Overshoot, at the leading edge of pulses, of up to 5% of the pulse amplitude at the middle of the signal element, is permitted, provided that such overshoot has, at half of its amplitude, a duration of less than 0,25 µs.

10.5.3.2 Nominal Pulse Amplitude

The nominal pulse amplitude of a ZERO shall be 750 mV, zero-to-peak.

A positive pulse (in particular a framing pulse) at the output ports of the PT and DPE is defined as a positive polarity of the voltage measured between access leads 4 to 5 and 3 to 6, respectively, see Figure 34.

10.5.4 Pulse Unbalance

The pulse unbalance, i.e. the difference between $\int U(t)dt$ for both positive and negative pulses, shall be ≤ 5%.

10.5.5 Voltage on Other Test Loads

10.5.5.1 Test Load of 400 Ω

A pulse (ZERO) shall conform to the limits of the mask shown in Figure 28 when the transmitter is terminated in a 400 Ω load.

10.5.5.2 Test Load of 5,6 Ω

The limit the current flow with two drivers having opposite polarities, the pulse amplitude (peak) with a 5,6 Ω load shall be ≤ 20% of the nominal pulse amplitude.

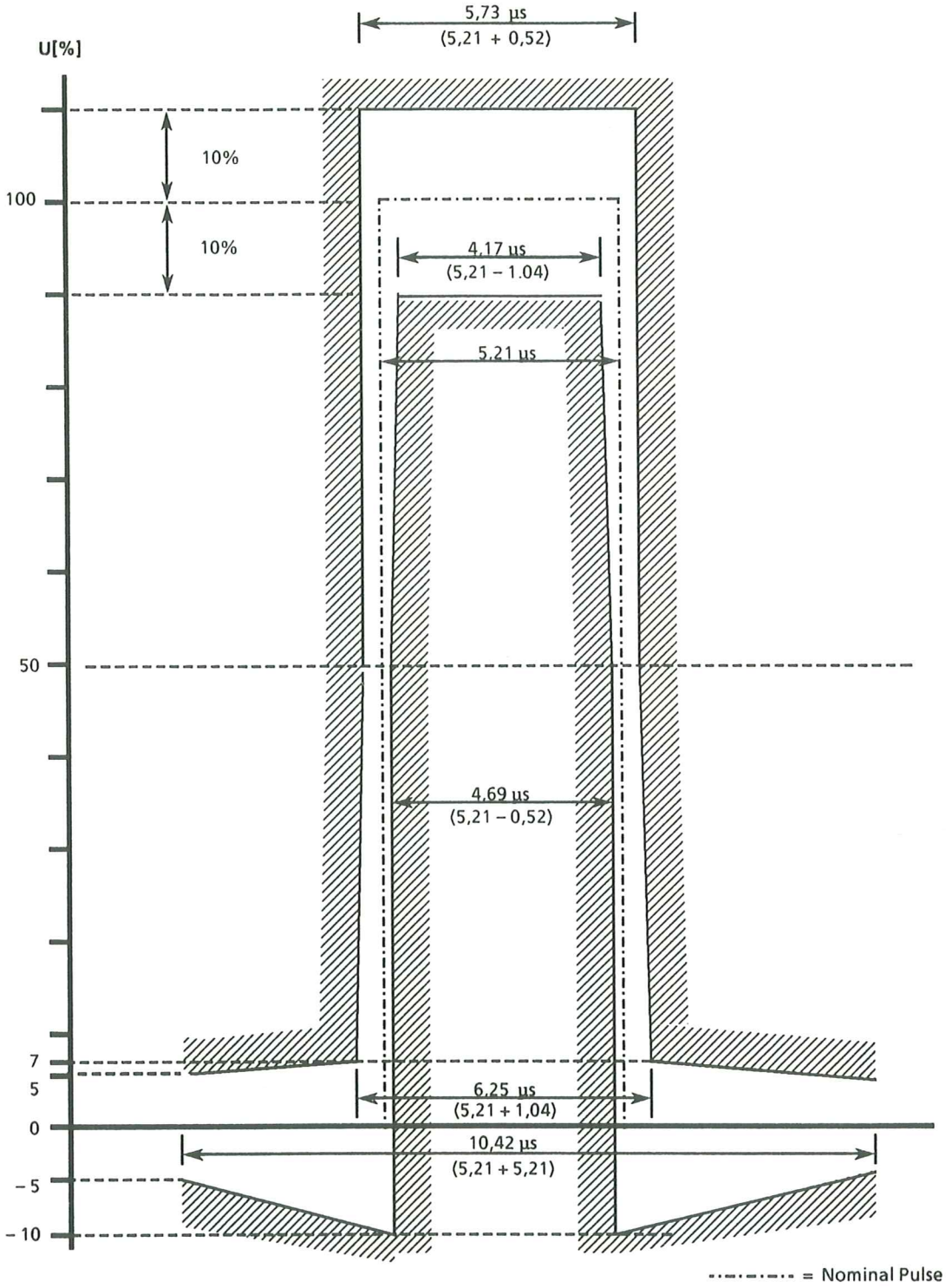


Figure 29 - DPE Output Pulse Mask

Note 33

For the clarity of presentation the above values are based on a pulse length of 5,21 µs. The precise value can be derived from the bit rate given in 10.1.

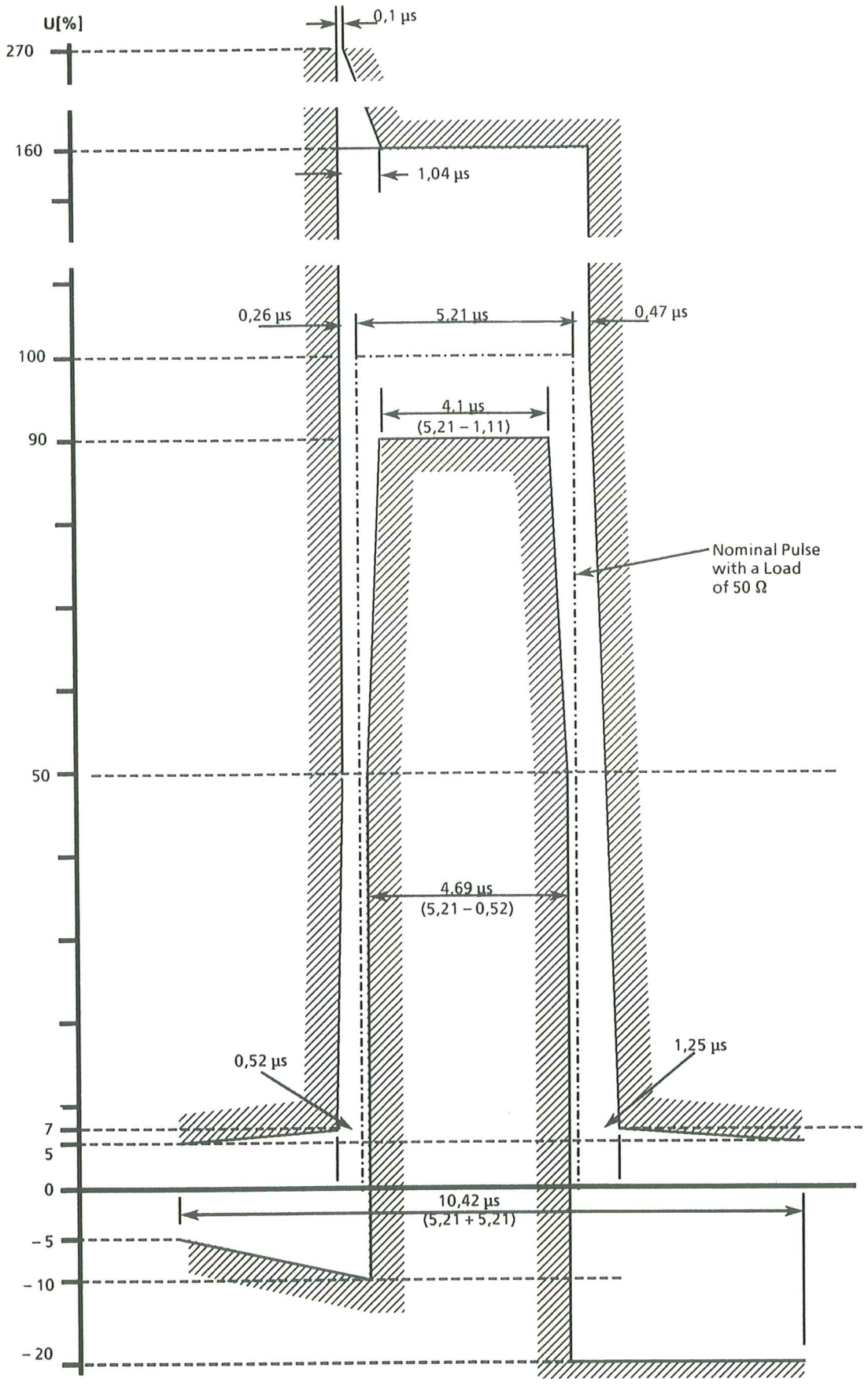


Figure 30 - DPE Output Pulse Mask on a Test Load of 400 Ω

Note 34

For the clarity of presentation the above values are based on a pulse length of 5,21 µs. The precise value can be derived from the bit rate given in 10.1.

10.5.6 Unbalance about Earth

The following requirements shall apply under all possible power feeding conditions, under all possible connections of the equipment to ground, and with two 100 Ω terminations across the transmit and receive ports.

10.5.6.1 Longitudinal Conversion Loss

The Longitudinal Conversion Loss (LCL) shall be measured in accordance with CCITT Rec. G.117, see Figure 30.

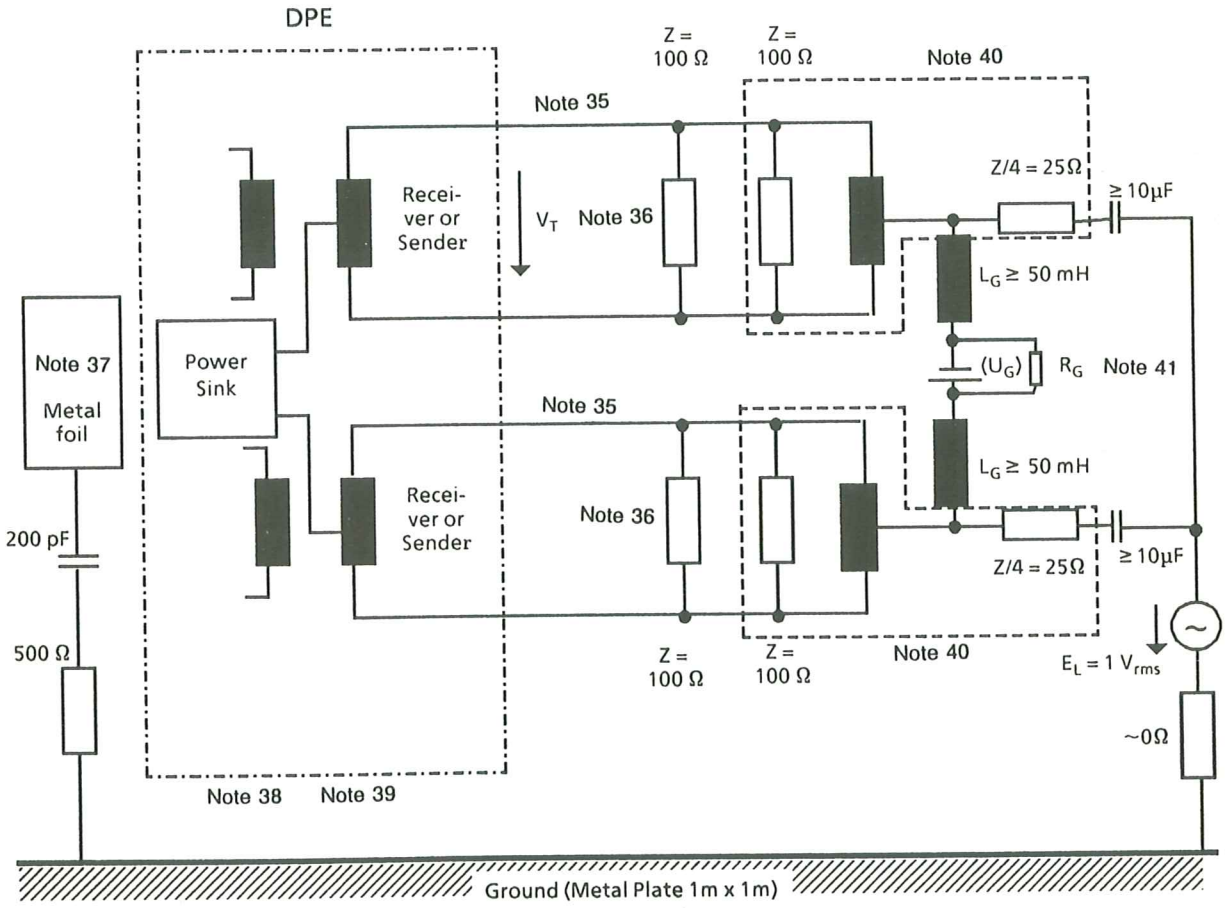


Figure 31 - Receiver Input or Sender Output Longitudinal Conversion Loss

Note 35

The interconnecting cord shall lie on the metal plate.

Note 36

This resistor forms the terminating resistor.

Note 37

Hand imitation; a thin metallic foil with approximately the size of a hand.

Note 38

DPEs with a metallic housing shall have a galvanic connection to the metal plate. DPEs with non-metallic housings shall be placed on the metal plate.

Note 39

The power cord for mains powered DPEs shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

Note 40

This circuit provides a transversal termination of 100 Ω and a balanced longitudinal termination of 25 Ω. Any equivalent circuit as given in CCITT Rec. G.117 and O.121 is also acceptable.

Note 41

If there is no power source 1 in the PT, R_G and L_G are not required.

The longitudinal conversion loss LCL, expressed in dB, is defined as:

$$LCL = 20 \cdot log_{10} \left| \frac{E_L}{V_T} \right| \; dB$$

The voltages V_T and E_L shall be measured within the frequency range from 10 kHz up to 1 MHz by employing selective test equipment.

The measurements shall be carried out in the states:

- F3 DEACTIVATED (receiver and sender)
- F1 INACTIVE (receiver and sender)

The longitudinal conversion loss shall be in the range

i)	between 10 kHz and 300 kHz incl.	≥ 54 dB
ii)	from over 300 kHz to 1 MHz incl.	minimum value of range i), decreasing with ≤ 20 dB/decade.

10.5.6.2 Output Signal Balance

The Output Signal Balance (OSB) shall be measured (see CCITT Rec. G.117) in accordance with Figure 31 by considering the power feeding and two 100 Ω terminations at each port.

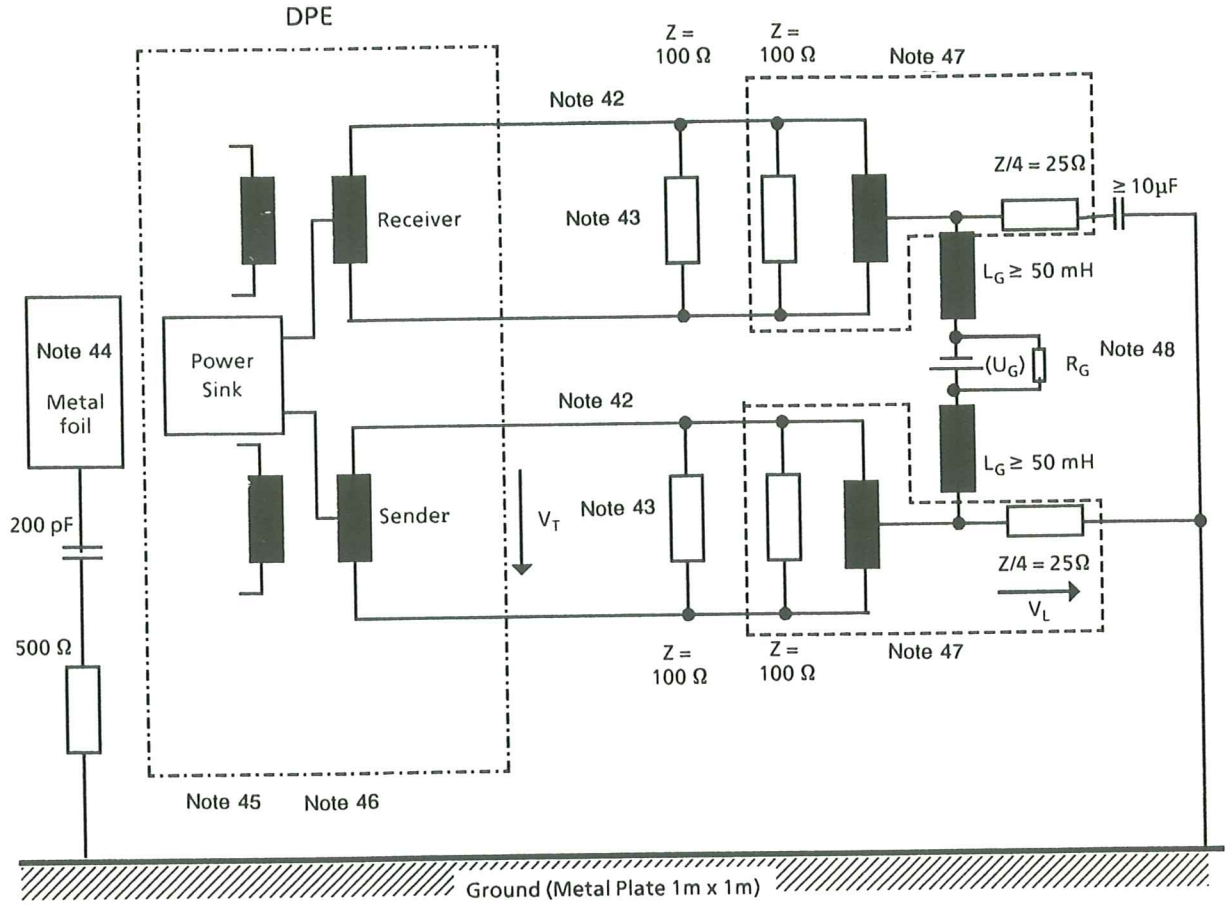


Figure 32 - Sender Output Unbalance about Earth

Note 42

The interconnecting cord shall lie on the metal plate.

Note 43

This resistor forms the terminating resistor.

Note 44

Hand imitation; a thin metallic foil with approximately the size of a hand.

Note 45

DPEs with a metallic housing shall have a galvanic connection to the metal plate. DPEs with non-metallic housings shall be placed on the metal plate.

Note 46

The power cord for mains powered DPEs shall lie on the metal plate and the earth protective wire of the mains shall be connected to the metal plate.

Note 47

This circuit provides a transversal termination of 100 Ω and a balanced longitudinal termination of 25 Ω. Any equivalent circuit as given in CCITT Rec. G.117 and O.121 is also acceptable.

Note 48

If there is no power source 1 in the PT, R_G and L_G are not required.

The output signal balance, expressed in dB, is defined as:

$$OSB = 20 \cdot log_{10} \left| \frac{V_T}{V_L} \right| dB$$

The voltages V_T and V_L shall be measured within the frequency range of 10 kHz to 1 MHz by employing selective test equipment. The measuring shall be carried out in a maintenance state under the normal power consumption condition, see 11.2. The pulse patterns should be all ZEROs. However, for the purpose of demonstrating the compliance of equipment, it is sufficient to measure the output signal unbalance about earth with a pulse pattern of continuous frames with at least the B1 and the B2 channels containing all ZEROs.

The output signal balance shall be in the ranges

i)	at 96 kHz	≥ 54 dB
ii)	from over 96 kHZ to 1 MHz	minimum value of range i), decreasing with ≤ 20 dB/decade.

10.6 DPE Input Characteristics

10.6.1 DPE Receiver Input Impedance

DPEs shall meet the requirements specified in 10.5.1.

10.6.2 Receiver Sensitivity, Noise and Distortion Immunity

DPEs shall receive without errors (for a period of at least one minute) an input with a pseudo random sequence (word length ≥ 511 bits) in all information channels (combination of B-channel, D-channel, and , if applicable, the D-echo channel).

The receiver shall operate with the input signals conforming to the waveforms specified in 10.2.1. For the waveforms depicted in Figures 22 to 24, DPEs shall operate with the input signals having any amplitude in the range of + 1,5 dB to -3,5 dB relative to the nominal amplitude of the transmitted signal as specified in 10.5.3.2. For signals conforming to the waveform depicted in Figure 21, operation shall be accomplished with any amplitude in the range of + 1,5 dB to - 7,5 dB relative to the nominal amplitude of the transmitted signal as specified in 10.5.3.2. Additionally, the DPEs shall operate with sinuosidal signals having an amplitude of 100 mV peak-to-peak at frequencies of 200 kHz and 2

MHz superimposed individually on the input signals having the waveform shown in Figure 21.

10.6.3 Unbalance about Earth

The Longitudinal Conversion Loss shall be measured by considering the power feeding and two 100 Ω terminations at each port as indicated in Figure 31 (see also CCITT Rec. G.117).

i)	between 10 kHz to 300 kHz	≥ 54 dB
ii)	from over 300 kHz to 1 MHz	minimum value of range i), decreasing with ≤ 20 dB/ decade.

10.7 Isolation from external Voltages

See Standard ECMA-83 and Technical Report ECMA TR/35.

10.8 Interconnecting Media Characteristics

The interconnecting media shall use twisted pairs; their longitudinal conversion loss at 96 kHz shall be ≥ 43 dB.

10.9 Standard ISDN Basic Access TE Cord

A connection cord for use with a DPE designed for connection with a "standard ISDN basic access TE cord" shall have a maximum length of 10 m and shall conform to 10.9.1 and 10.9.2.

10.9.1 Cords with a maximum Length of 7 m

The maximum capacitance of pairs for transmit and receive functions shall be less than 300 pF.

The characteristic impedance of pairs used for transmit and receive functions shall be ≥ 75 Ω at 96 kHz.

The crosstalk loss at 96 kHz between any pair and a pair to be used for transmit or receive functions shall be greater than 60 dB with terminations of 100 Ω.

The resistance of an individual conductor shall not exceed 3 Ω.

Cords shall be terminated at both ends in plugs, and individual conductors shall be connected to the same contact in the plugs at each end.

10.9.2 Cords having a Length greater than 7 m

Cords shall conform to the requirements specified in 10.9.1, except that a capacitance of 350 pF is permitted.

10.10 Cords forming Part of the DPE

DPEs may be designed such that they include a connection cord which is part of the DPE. In this case the requirement for a standard "ISDN basic access TE cord" do not apply.

Note 49

When the cord is not part of the DPE, its capacitance will still form part of the overall capacitance of 800 pF of the overall assembly (see 10.5.1).

11. POWER FEEDING

11.1 Reference Configuration

Although an 8-pole connector is to form a universal CCITT S_0 interface (see CCITT Rec. I.430), the ECMA reference configuration uses the four access leads 3 to 6 only, as depicted in Figure 32. The use of the leads 1, 2, 7, and 8 is outside the scope of this Standard.

Note 50

The numbering of the leads does not imply any assumption on pin allocation of physical connectors.

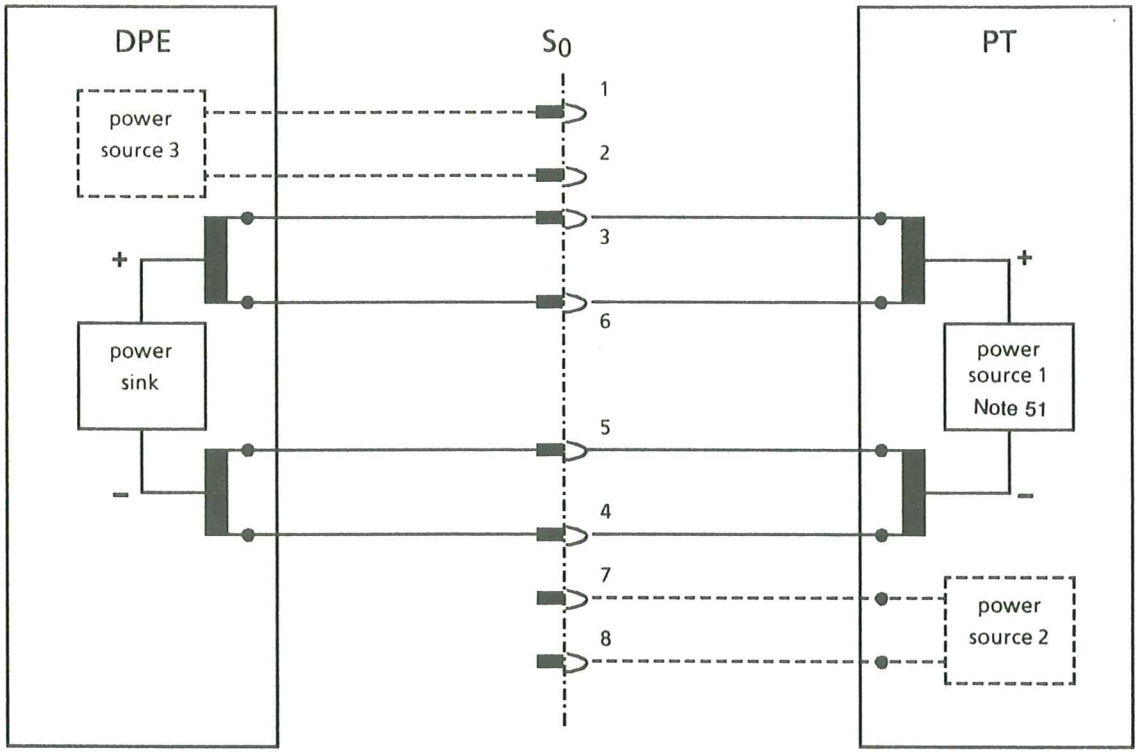


Figure 33 - Power Feeding via the S_0 interface

Note 51

The polarity of the voltage of power source 1 refers to the normal powering condition. Under restricted conditions the polarity is reversed.

11.1.1 Functions Specified for the Access Leads

The access leads 3 to 6, used for the bi-directional transmission of the digital signal, may provide a phantom circuit for power transfer from the PSN to the DPE (power source 1/power sink).

11.1.2 Provision of Power Sources

The DPE (power sink) may be powered by power source 1 or by power source 3.

- Power source 1 may not always be provided.

Note 52

A terminal that is to be portable (for example from PSN to PSN, country to country) cannot rely exclusively on phantom power for its operations.

- Power source 2 is outside the scope of this Standard.

- Power source 3 is outside the scope of this Standard.

11.2 Power available at the DPE from Power Source 1

With power source 1, two situations are considered, "normal" and "restricted".

When the PT enters a state where it is only able to supply restricted power, this will be indicated by reversing the polarity of power source 1. In this condition only a reduced set of terminal functions is allowed to consume power from power source 1.

Under normal conditions, the maximum voltage at the interface of a TE will be 40 V + 5% (42 V) and the minimum voltage will be 40 V - 40% (24 V), when drawing the maximum permitted power consumption of 1 W.

Under restricted conditions, the nominal value of voltages at the inputs of TEs (from power source 1) will be 40 V and the tolerance will be + 5% and - 20%, when drawing a power of up to 400 mW (380 mW for a designated TE and 20 mW for other TEs).

11.3 Power Source 1 Consumption

The different values concerning power consumption from source 1 are summarized in Table 7.

Powered from	Type	Condition	State	Maximum Consumption
Power Source 1	Designated or Non-Designated	Normal	ACTIVE	1 W
			DEACTIVATED	100 mW
			Local Action	1 W Note 53
	Designated	Restricted	ACTIVE	380 mW
			DEACTIVATED	25 mW
			Local Action	380 mW Note 53
	Non-Designated		Any	0 mW
Locally (but using power source 1 for sensing)	Designated or Non-Designated	Restricted	Any	3 mW

Table 7 - Summary of the different possible Power Source 1 Consumptions

Note 53

Subject to the provision of the corresponding amount of power by power source 1.

11.3.1 Normal Power Conditions

Under normal power conditions and when involved in a call, a DPE which draws power from power source 1 shall draw no more than 1 W. When a DPE

is not involved in a call, but is in the ACTIVATED state, is shall not draw more than 380 mW.

When a DPE is in the DEACTIVATED state, it shall draw no more than 100 mW from power source 1.

11.3.2 Restricted Power Conditions

11.3.2.1 Power available to a TE "designated" for restricted power operation

A TE, which is permitted to draw power from power source 1 under restricted power conditions, shall consume no more than 380 mW.

Under restricted power conditions and in the DEACTIVATED state, a designated DPE may consume up to 25 mW from power source 1, e.g. only to maintain a line activity detector. The value of the power-down mode consumption shall be ≤ 25 mW in order to enable retainment of its Terminal Endpoint Identifier value (TEI value, see ECMA-105).

11.3.2.2 Power available to a TE "not-designated" for restricted Power Operation

Non-designated, locally powered DPEs shall consume no more than 3 mW from power source 1 under restricted power conditions, e.g. to use a device for detecting restoration of the normal power condition.

11.4 Current transients

The rate of change of current drawn by a DPE (e.g. when being connected or as a result of a polarity change for indication of the restricted condition) shall not exceed 5 mA/µs.

12. PHYSICAL CHARACTERISTICS

12.1 Connectors

The connectors (including their pin allocation) shall be as defined for use at the ISDN basic user-to-network interface (at the S reference point) in ISO DIS 8877.

12.2 Connection Cord

For the electrical characteristics of the connection cord see 10. Other characteristics are specified below.

12.2.1 Use of the Access Leads

As shown in Figure 34, the PSN will provide a one-to-one mapping between the outlets of the S_0 female connector(s) and its PT (however, see 6.3 for possible polarity reversal). The connection cord shall provide four access leads fitting to the leads 3 to 6 of the PSN wiring.

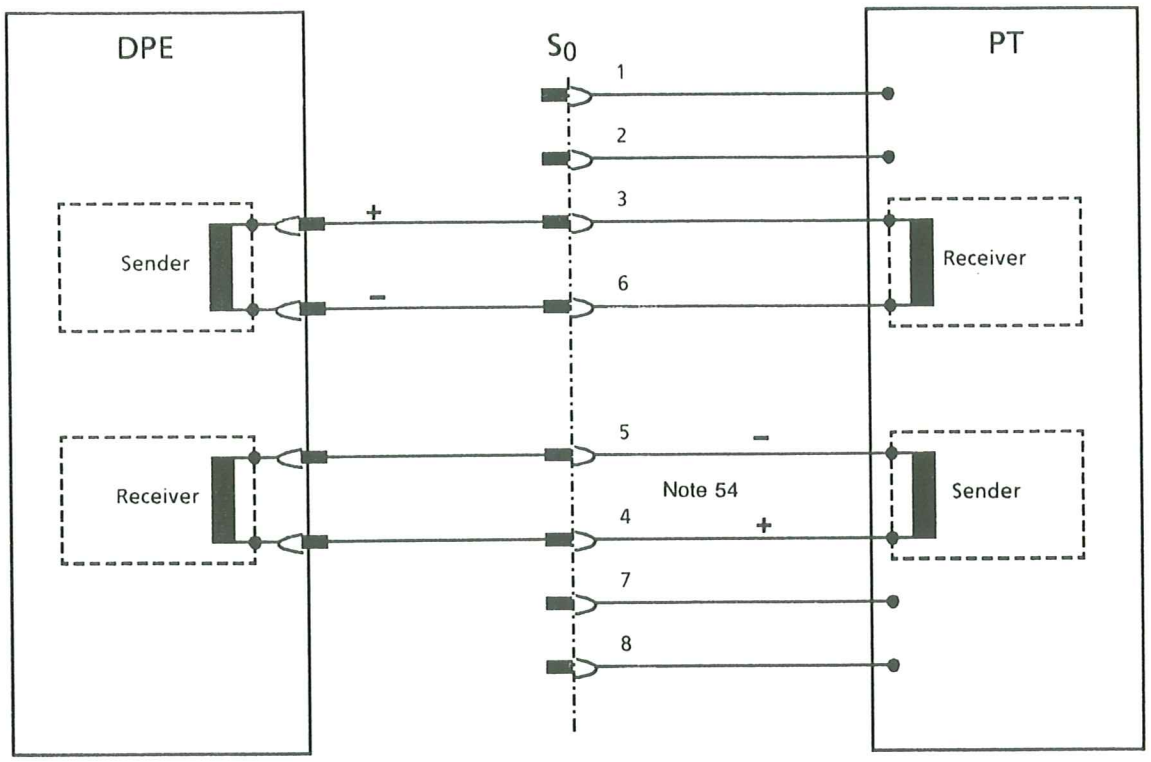


Figure 34 - Use of the S_0 Interface Access Leads

Note 54

Due to possible reversion of the two-wire interchange circuit (see 6.3), the bits may be received with opposite polarity.

12.2.2 Signal Polarity of the Access Leads

A positive pulse (e.g. a framing pulse) transmitted by the DPE is defined with a positive voltage of the PSN access lead 3 relative to PSN access lead 6, see Figure 34.

If the wiring polarity is maintained, a positive pulse (e.g. a framing pulse) received by the DPE will occur as a positive voltage between PSN access leads 4 and 5, see Figure 34.

LIST OF ACRONYMS

AMI	Alternate Mark Inversion
DPE	Data Processing Equipment
IWU	Interworking Unit
LCL	Longitudinal Conversion Loss
MPH-AI	Management/Physical Layer Activate Indication
MPH-AR	Management/Physical Layer Activate Request
MPH-DI	Management/Physical Layer Deactivate Indication
MPH-DR	Management/Physical Layer Deactivate Request
MPH-EI	Management/Physical Layer Error Indication
MPH-II	Management/Physical Layer Information Indication
MPH-LAI	Management/Physical Layer Loop Activation Indication
MPH-LAR	Management/Physical Layer Loop Activation Request
MPH-LDI	Management/Physical Layer Loop Deactivation Indication
MPH-LDR	Management/Physical Layer Loop Deactivation Request
MULDEX	Multiplexer/Demultiplexer
OSB	Output Signal Balance
PSN	Private Switching Network
PH-AI	Physical Layer Activate Indication
PH-AR	Physical Layer Activate Request
PH-DI	Physical Layer Deactivate Indication
PT	PSN Termination
SDL	Specification and Description Language
TE	Terminal Equipment