ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-104

PHYSICAL LAYER AT THE PRIMARY RATE ACCESS INTERFACE BETWEEN DATA PROCESSING EQUIPMENT AND PRIVATE CIRCUIT SWITCHING NETWORKS

September 1985

Free copies of this document are available from ECMA,
European Computer Manufacturers Association
114 Rue du Rhône – 1204 Geneva (Switzerland)

ECMA

EUROPEAN COMPUTER MANUFACTURERS ASSOCIATION

STANDARD ECMA-104

PHYSICAL LAYER AT THE PRIMARY RATE ACCESS INTERFACE BETWEEN DATA PROCESSING EQUIPMENT AND PRIVATE CIRCUIT SWITCHING NETWORKS

September 1985

BRIEF HISTORY

This Standard ECMA-104 is one of a series of standards for the connection of data processing equipment to private circuit switching networks.

It uses the ISDN concepts as developed by CCITT and it is also within the framework of standards for open systems interconnection as defined by ISO 7498 and within the Technical Report ECMA TR/24. It is based on the practical experience of ECMA member companies and the results of their active and continuous participation in the work of ISO, CCITT and various national standardization bodies in Europe and in the USA. It represents a pragmatic and widely based consensus.

This Standard ECMA-104 specifies the Physical Layer of the interface as presented by the data processing equipment. Where appropriate, assumptions of the interface as presented by the private circuit-switching network are also indicated.

This Standard has been accepted by the General Assembly of ECMA on June 13, 1985.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont'd)

1 Scope and Field of Application

This ECMA Standard defines the Physical Layer characteristics of the primary rate access interface between data processing equipment (DPE) and private circuit switching networks (PCSN). The interface concerned is at the S reference point as defined in CCITT Recommendation I.411. The reference configuration for the interface is given in Figure 1.

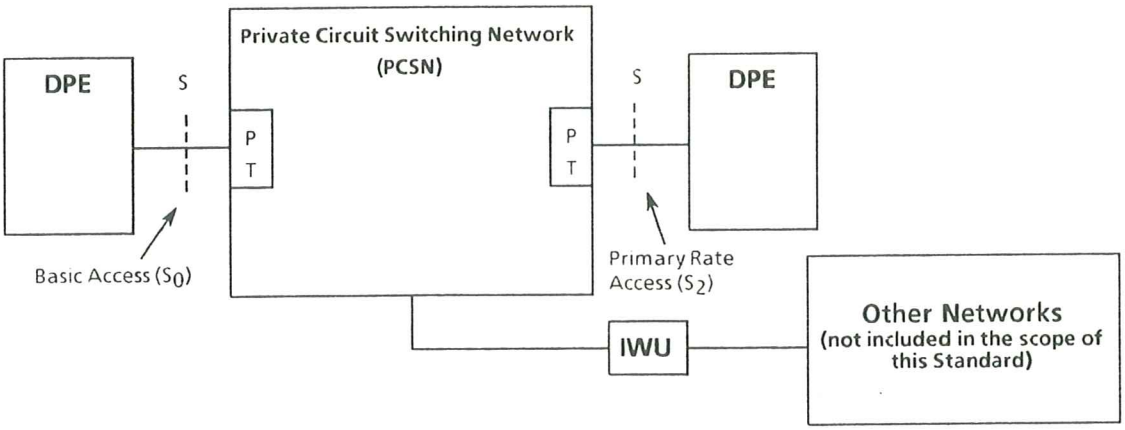


Figure 1 - Reference Configuration for S_0 and S_2 Interfaces

The Standard is based on CCITT Recommendation I.431.

2 References

CCITT Recommendation G.701	Vocabulary of digital transmission and multiplexing, and pulse code modulation (PCM) terms
CCITT Recommendation G.703	Physical/electrical characteristics of hierarchical digital interfaces
CCITT Recommendation G.704	Functional characteristics of interfaces associated with network nodes
CCITT Recommendation G.732	Characteristics of primary PCM multiplex equipment operating at 2048 kbit/s
CCITT Recommendation G.736	Characteristics of synchronous digital multiplex equipment operating at 2048 kbit/s
CCITT Recommendation I.112	Vocabulary of terms for ISDNs
CCITT Recommendation I.320	ISDN protocol reference model
CCITT Recommendation I.411	ISDN user-network interfaces - reference configurations
CCITT Recommendation I.412	ISDN user-network interfaces - interface structures and access capabilities
CCITT Recommendation I.431	Primary rate user-network interface - layer 1 specification
CCITT Recommendation X.200	Reference model of Open Systems Interconnection for CCITT applications
CCITT Recommendation X.211	Physical layer service definitions of open system interconnections for CCITT applications
CCITT Recommendation Z.101..104	Recommendations on the functional specification and description language (SDL)

Note: For the CCITT Recommendations listed above their Red Book versions apply.

3 Definitions

A basic vocabulary of terms can be found in CCITT Recommendations G.701 and I.112. In addition,the following definitions of terms are used in this Standard:

B-Channel
The B-channel is a 64 kbit/s access channel with bit and octet timing. It is used to carry user data in both directions of transmission between DPEs connected over a PCSN.

Co-directional interface
The co-directional interface is an interface across which the signals to be transferred and their associated timing signals are transmitted in the same direction.

D-Channel
The D-channel is a 64 kbit/s access channel. It is used to carry signalling and other information in both directions of transmission between a DPE and the PCSN.

Data Processing Equipment (DPE)
Specific type of terminal equipment, exclusively or mainly used to process data (in contrast to a voice-only terminal).

Interworking Unit (IWU)
An IWU is the function needed for a PCSN to interwork with other networks.

Layer Service
This term is defined in the ISO Reference Model on Open Systems Interconnections (ISO 7498).

Private Circuit Switching Network (PCSN)
An entity providing circuit switching funtions with full digital transmission capability. It is operated by the user and located on his premises to cover the communications needs in his domain. It is bounded by S interfaces.

PCSN Termination (PT)
The termination of a PCSN at the S reference point.

S_0 Interface
The S_0 interface is the basic access interface at the S reference point (see CCITT Recommendation I.411) operating at a physical bit rate of 192 kbit/s. It provides access to two B-channels and one D-channel (2B + D). The S_0 interface forms one of the user access points to a PCSN.

S_2 Interface
The S_2 interface is the primary rate access interface at the S reference point (see CCITT Recommendation I.411) operating at a physical bit rate of 2048 kbit/s. It provides access to 30 B-channels and one D-channel (30B + D). The S_2 interface forms one of the user access points to a PCSN.

Specification and Description Language (SDL)
The specification and description language according to CCITT Recommendations Z.101...Z.104.

Terminal Equipment (TE)
A general term to designate any terminal (voice or data processing or combination of both) connected to a PCSN at the S_0 or at the S_2 interface.

Time-Slot
A time-slot designates any cyclic time interval that can be recognized and defined uniquely.

4. Layer Service Characteristics

General information on layer services and layered protocols can be found in CCITT Recommendation X.200 and ISO 7498.

4.1 Layer Services required from the Physical Medium

The Physical Layer of the S_2 interface requires a balanced metallic transmission medium for each direction of transmission, capable of supporting 2048 kbit/s.

4.2 Layer Services provided to the Data Link Layer

The Physical Layer provides the following services to the Data Link Layer:

4.2.1 Transmission capability by means of appropriately encoded bitstreams, for 30 B-channels and the D-channel.

4.2.2 Timing and synchronization functions.

4.2.3 The signalling capability and procedures and the necessary functions at the Physical Layer to enable the maintenance functions to be performed.

4.2.4 An indication to the higher layers and the Management Entity about the status of the Physical Layer.

4.3 Primitives between the Physical Layer and other Entities

4.3.1 The primitives used between the Physical Layer and other entities are:

PH-AI, MPH-AI	see 8.2.1.4
PH-DI, MPH-DI	see 8.2.1.5
MPH-EI	see 8.2.1.6
PH-DATA-I/R	PHYSICAL LAYER DATA INDICATION/REQUEST These primitives are used to indicate the arrival of a message unit or to request that a message unit be sent.

4.3.2 These primitives represent the logical exchange of information and control between the Physical Layer, the Data Link Layer and the Management Entity, see Figure 2. They do not specify nor constrain the implementation of entities or interfaces. For a description of the syntax and use of the primitives refer to CCITT Recommendation X.211.

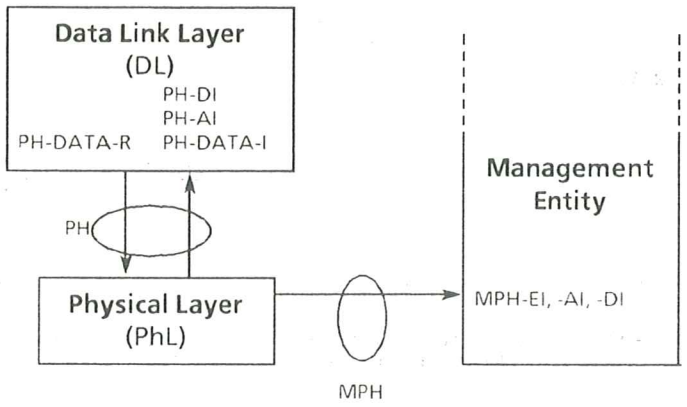


Figure 2 - Physical Layer Primitives

4.3.3 The values of the primitives are defined in Table 1. Relevant detailed description of the primitives and their procedures is given in 8.2.1

5 Mode of Operation

The characteristics of the Physical Layer interface allow only for the point-to-point mode of operation. This implies that only one source (transmitter) and one sink (receiver) are active at the interface at any time in each direction of transmission.

Generic Name	Function			Parameter		Message Unit Contents	
	Request	Indication	Response	Priority Indicator *(Note 2)*	Message Unit		
PH-DATA	x *(Note 1)*	x	–	–	x	Data Link Layer peer-to-peer message	↑ between the Physical and the Data Link Layer ↓
PH-ACTIVATE	– *(Note 2)*	x	–	–	–		
PH-DEACTIVATE	– *(Note 2)*	x	–	–	–		
MPH-ACTIVATE	– *(Note 2)*	x	–	–	–		↑ between Physical Layer and Management Entity ↓
MPH-DEACTIVATE	–	x	–	–	–		
MPH-ERROR	–	x *(Note 3)*	–	–	x	Additional Information	

Note 1:
PH-DATA-REQUEST implies underlying negotiation between the physical and the data link layer for the acceptance of the data.

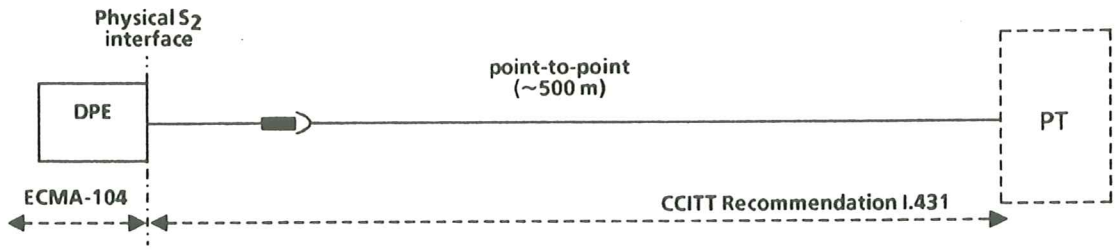
Note 2:
This function/parameter may be used by the Data Link Layer or the Management Entities for the purpose of consistency with the basic access procedures (see ECMA PhLx1). If they are provided they will cause no activity other than indication of the status of the Physical Layer.

Note 3:
The INDICATION includes the type of the error.

Table 1 - Values of Physical Layer Primitives

6 Wiring Configuration

Figure 3 shows the general reference configuration for the wiring at user premises which is a point-to-point wiring configuration. The electrical characteristics of the S_2 interface are determined on the basis of such wiring configuration.



Note:
The length depends on the electrical characteristics of the cabling and the value indicated is given for tutorial background information only.

Figure 3 - Reference Configurations for Primary Rate Access Wiring at the User's Premises and Location of the S_2 Interface

6.1 Point-to-Point Configuration

Point-to-point wiring configuration implies that only one source (transmitter) and one sink (receiver) are interconnected via an interchange circuit.

6.2 Wiring Polarity Integrity

The two wires of each interchange circuit pair may be reversed.

6.3 Location of the Interface

The S_2 interface is physically located at the DPE. It consists of a connector as indicated in Chapter 12. Any sockets and connecting cords are considered to be part of the PCSN wiring.

7 Functional Characteristics

7.1 Interface Functions

7.1.1 Bit Timing
This function provides bit (signal element) timing at 2048 kbit/s to enable DPE and PT to recover information from the aggregate bit stream.

7.1.2 Octet Timing
This function provides 8 kHz octet timing for the PT and DPE.

7.1.3 Frame Alignment
This function provides information to enable PT and DPE to recover the time division multiplexed channels.

7.1.4 B-Channel
This function provides an access channel with a bit rate of 64 kbit/s for each direction of transmission, as defined in CCITT Recommendation I.412.

7.1.5 D-Channel
This function provides one D-channel with bi-directional transmission a bit rate of 64 kbit/s, as defined in CCITT Recommendation I.412.

7.2 Interchange Circuits
Two interchange circuits, one for each direction of transmission, are used to transfer digital signals across the interface. All functions described in 7.1 are combined into two composite digital signals, one for each direction of transmission.

7.3 Frame Structure
In both directions of transmission, data are grouped into frames of 256 bits (numbered 1 to 256) resulting from 32 time slots (numbered 0 to 31) of 8 bits each (numbered 1 to 8).

7.3.1 Bit Rate
The nominal transmitted bit rate at the interface is 2048 kbit/s in both directions of transmission.

7.3.2 Time-Slot Assignment
The time-slot assignment is depicted in Figure 4.

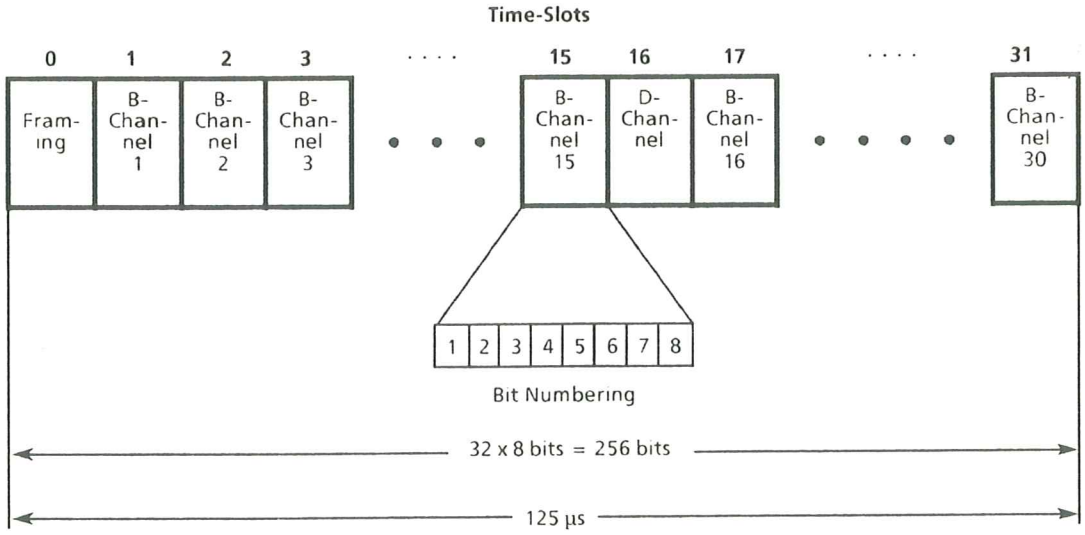


Figure 4 - Time-Slot Assignment

7.3.2.1 Time-Slot 0
Time-slot 0 conveys frame alignment information (see 7.3.2.3), remote alarm indication (see 8.2) and, optionally, information for a cyclic redundancy check procedure (see 7.4). The content varies alternately, ie. between odd and even numbered frames, see Table 2.

Alternate Frames	Bit Number in Time-Slots 0							
	1	2	3	4	5	6	7	8
Even numbered Frames	S_i (Note 1)	0	0	1	1	0	1	1
Odd numbered Frames	S_i (Note 1)	1 (Note 2)	A (Note 3)	S_n (Note 4)	S_n (Note 4)	S_n (Note 4)	S_n (Note 4)	S_n (Note 4)

Note 1:
The S_i-bit is either fixed to "1" or, optionally, used as described in 7.4.
Note 2:
This bit is fixed to "1" to assist in avoiding simulations of the frame alignment signal.
Note 3:
The A-bit is used for remote alarm indication. In an alarm condition, it is set to "1".
Note 4:
The S_n-bits are spare bits; when not used, they shall be fixed at "1".

Table 2 - Bit Allocation in Channel Time-Slots 0

7.3.2.2 Time-Slots 1 to 31

Time-slots 1 to 31 are bit transparent. The bit allocation depends on the higher layer protocols.

Time-slots 1 to 15 and 17 to 31 are allocated to the B-channels while time-slot 16 is allocated to the D-channel.

7.3.2.3 Frame Alignment Information

The frame alignment signal is coded 0011011 and occupies bit positions 2 to 8 in time-slots 0 of all even numbered frames.

Bit 2 of the odd numbered frames is fixed to "1" to assist in avoiding simulations of the frame alignment signal.

7.4 Cyclic Redundancy Check

The cyclic redundancy check is optional. When it is provided, it shall be based on the special use of bit 1 of time-slots 0 and follow the CRC4 procedure as detailed in CCITT Recommendation G.704. It will provide additional protection against simulation of the frame alignment strategy and/or enhanced error monitoring capability.

7.5 Line Code

According to CCITT Recommendation G.703, the HDB3 line code is used at the S_2 interface. The coding of a binary signal into an HDB3 signal is done according to the following rules, see Figure 5:

I. The HDB3 signal is pseudo-ternary, the three states are denoted $B+$, $B-$ and *0*.

II. Binary ZEROs are coded as 0 in the HDB3 signal. For strings of binary ZEROs, however, special rules apply, see IV below.

III. Binary ONEs are coded alternately as $B+$ and $B-$ in the HDB3 signal ("alternate ONE inversion"). Violations of the rule of alternate ONE inversion are introduced when coding strings of four binary ZEROs, see IV below.

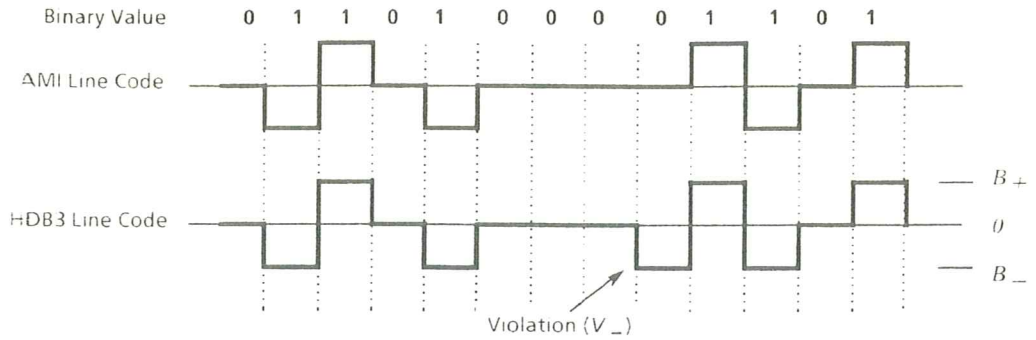
IV. Strings of four binary ZEROs are coded according to the following rules:

a. The first binary ZERO of a string is coded as a *0* if the preceding *B* of the HDB3 signal has a polarity opposite to the polarity of the preceding violation and is not a violation by itself; it is coded as *B*, ie. not a violation (ie. $B+$ or $B-$), if the preceding *B* of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

This rule ensures that successive violations are of alternate polarity so that no DC component is introduced.

b. The second and the third ZERO of a string are always coded as *0*.

c. The last ZERO of a string of four is always coded as a *B*, the polarity of which is such that it violates the rule of alternate ONE inversion. Such violations are denoted $V+$ or $V-$, according to their polarity.



Note: The Figure shows the coding rule. The actual line signal provides a duty cycle of 50 %.

Figure 5 - AMI and HDB 3 Code (Example)

7.6 Timing considerations

The DPE derives its timing (bit, octet and frame) from the signal received from the PCSN and synchronizes its transmitted signals accordingly (ie. the timing signals provide a co-directional interface).

8 Interface Procedures

8.1 Frame Alignment Procedures

Frame alignment is assumed to have been lost when three or four consecutive frame alignment signals have been received with an error.

Frame alignment is assumed to have been recovered when the following sequence is detected:

- for the first time, the presence of the correct frame alignment signal:
- the absence of the frame alignment signal in the subsequent frame, detected by verifying that bit 2 in time-slot 0 is "1";
- for the second time, the presence of the correct frame alignment signal in the next frame.

Note:
To avoid the possibility of a state in which, due to the presence of an imitative frame alignment signal, no frame alignment can be achieved , the following procedure may be used:
When a valid frame alignment signal is detected in frame n, a check should be made to ensure that a frame alignment signal does not exist in frame n + 1, and also that a frame alignment signal exists in frame n + 2. Failure to meet one or both of these requirements should cause a new search to be initiated in frame n + 2.

8.2 Activation Procedure

The S_2 interface is considered to be active when it provides the B-channel and D-channel function, see 7.14 and 7.15. Since the procedures are symmetrical, the signals are used in both directions and the various states occur as well at the DPE side as at the PCSN side of the interface.

8.2.1 Definitions

8.2.1.1 Signals

The designation, the meaning and the coding of the Physical Layer signals across the S reference point are listed below.

INFO 0	consists of continuous HDB3 signal states 0, i.e. no pulses, see 7.5.
INFO 1	indicates that the DPE/PCSN is in an operational state. It consists of 256-bit frames structured as described in 7.3. It may provide operational data on the B-channels and on the D-channel.

INFO 2 conveys the remote alarm indication. It consists of 256-bit frames structured as described in 7.3. Bit 3 of time-slot 0 of odd numbered frames is set to "1", see Table 2.

8.2.1.2 DPE and PCSN Side States

F1 POWER OFF : The DPE/PCSN is powered off.

F2 REMOTE ALARM : The DPE/PCSN is receiving a remote alarm indication by means of INFO 2. The PCSN/DPE transmits INFO 1. The bit timing of the DPE is synchronized to that of the PCSN.

F3 ACTIVE : This is the normal active state when both sides transmit operational frames (INFO 1). The bit timing of the DPE is synchronized to that of the PCSN.

F4 LOCAL ALARM : The DPE/PCSN has detected a fault condition. An alarm indication is transmitted to the other side (INFO 2). The bit timing of the DPE may or may not be synchronized to that of the PCSN.

8.2.1.3 Activate Primitives

The following primitives are used in the activate procedure:

PH-AI ACTIVATE
MPH-AI INDICATION : These primitives are used by the Physical Layer to indicate that it is operational.

8.2.1.4 Deactivate Primitives

The following primitives are used in the deactivate procedures:

PH-DI DEACTIVATE
MPH-DI INDICATION : These primitives are used by the Physical Layer to indicate that it is not operational.

8.2.1.5 Error and Recovery Primitives

The following primitives should be used between the Physical Layer and the Management Entity:

MPH-EI MPH-ERROR INDICATION : This primitive includes the parameters "1", and"2":
MPH-EI 1 indicates an error report. The message unit contains the type of the fault. This can be
alarm indication from the remote end (receipt of INFO 2);
loss of incoming signal (receipt of INFO 0);
loss of frame alignment;
excessive bit error ratio.

MPH-EI 2 reports that no error condition now exists. This can be due to:
recovery from loss of frame alignment;
recovery from excessive bit error ratio.

Note1:
A detailed description of the fault conditions and recoveries can be found in CCITT Recommendation G.736, except for loss and recovery of frame alignment which can be found in CCITT Recommendation G.732.

Note 2:
During a fault condition the bit patterns in the B-channels and in the D-channel may be changed to all binary ONEs (this is known as Alarm Indication Signal, AIS, see CCITT Recommendation G.736).

8.2.2 State Transitions

The state transitions are shown in Table 3 in the form of a finite state matrix.

8.2.3 SDL Presentation of the Activation Procedure

Figures 6 to 8 show an SDL presentation of the activation procedure at the DPE side. The DPE is assumed to be on the left hand side of an interworking configuration. The activation procedure is partitioned into:

State Name	POWER OFF	REMOTE ALARM	ACTIVE	LOCAL ALARM
State Number	F1	F2	F3	F4
Info sent	INFO 0	INFO 1	INFO 1	INFO 2
Power switched off	/	(M)PH-EI1; F1	(M)PH-EI1 ; (M)PH-DI; F1	(M)PH-EI1; F1
Power switched on	F4	/	/	/
Receiving INFO 1 with non-excessive bit error ratio	/	(M)PH-EI2 ; (M)PH-AI; F3	–	(M)PH-EI2 ; (M)PH-AI; F3
Detecting a fault condition *(Note)*	/	(M)PH-EI1; F4	(M)PH-EI1 ; (M)PH-DI; F4	–
Receiving INFO 2 with non-excessive bit error ratio	/	–	(M)PH-EI1 ; (M)PH-DI; F2	(M)PH-EI1; F2

Legend: – No Change
/ Impossible Situation
P; Fn means: "Issue primitive P and then go to state Fn"

Note :
This fault condition can be:
loss of framing,
loss of bit timing,
INFO 1 with excessive bit error ratio,
INFO 2 with excessive bit error ratio.

Table 3 - Finite State Matrix on the Activation / Deactivation Procedure of the Physical Layer at the DPE or the PCSN Side

Activation and Recovery
Detection and treatment of fault conditions
Loss of power

The Physical Layer signals are continuous signals. An (external) output symbol indicates that the transmission of such signal is to be started. The transmission of this signal ends when it is replaced by another signal to be sent in the same direction. An (external) input symbol indicates that an incoming signal has arrived.

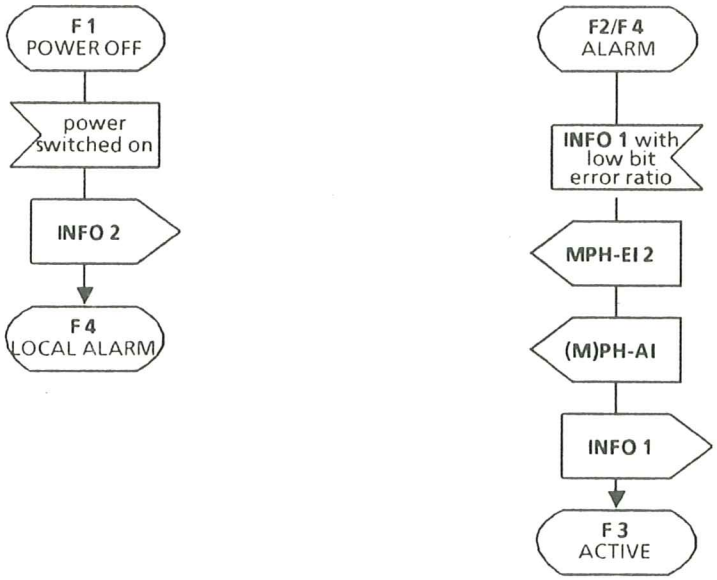
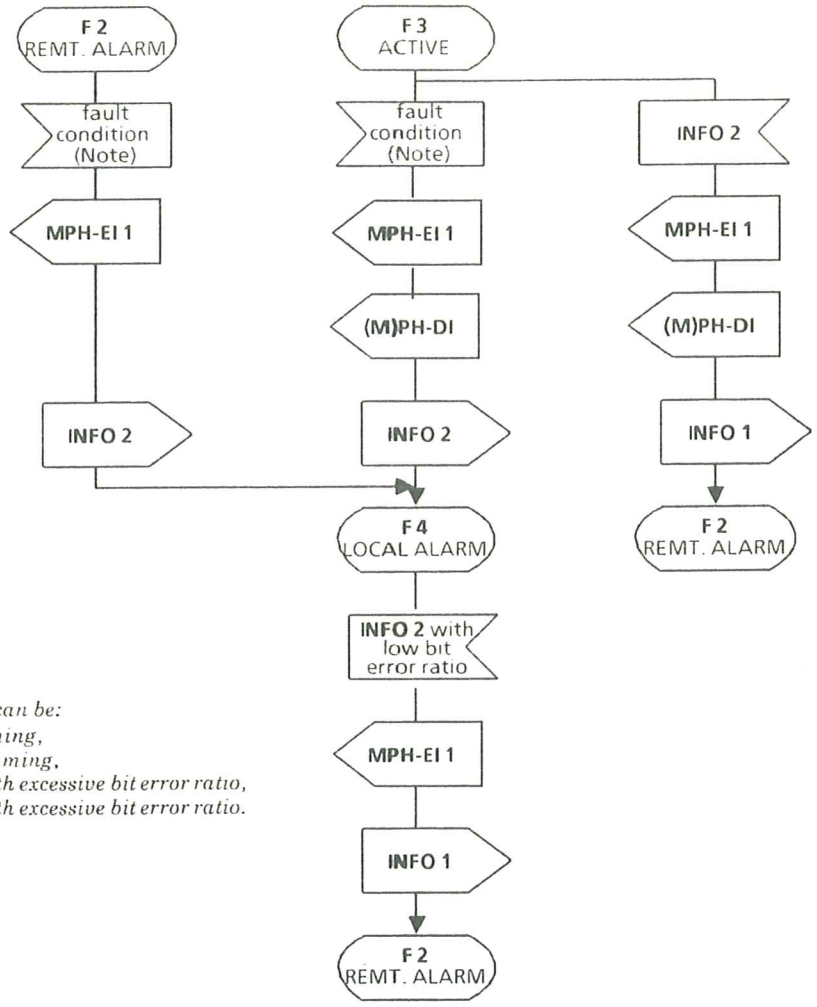


Figure 6 - Activation and Recovery Procedure



Note:
This fault condition can be:
loss of framing,
loss of bit timing,
INFO 1 with excessive bit error ratio,
INFO 2 with excessive bit error ratio.

Figure 7 - Detection and Treatment of Fault Condition

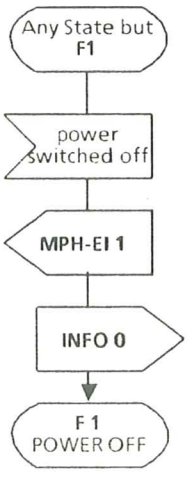


Figure 8 - Loss of Power

8.3 Idle Channel Code on B-Channels

A DPE shall send binary ONEs in any B-channel which is not used. This is the responsibility of higher layers.

9 Provisions for Physical Layer Maintenance

The Physical Layer shall provide the following maintenance facilities:

9.1 Test Loops

Six test loops, Loops A1, A3 and A4 and Loops B1, B3 and B4, can be activated, see Figure 9.

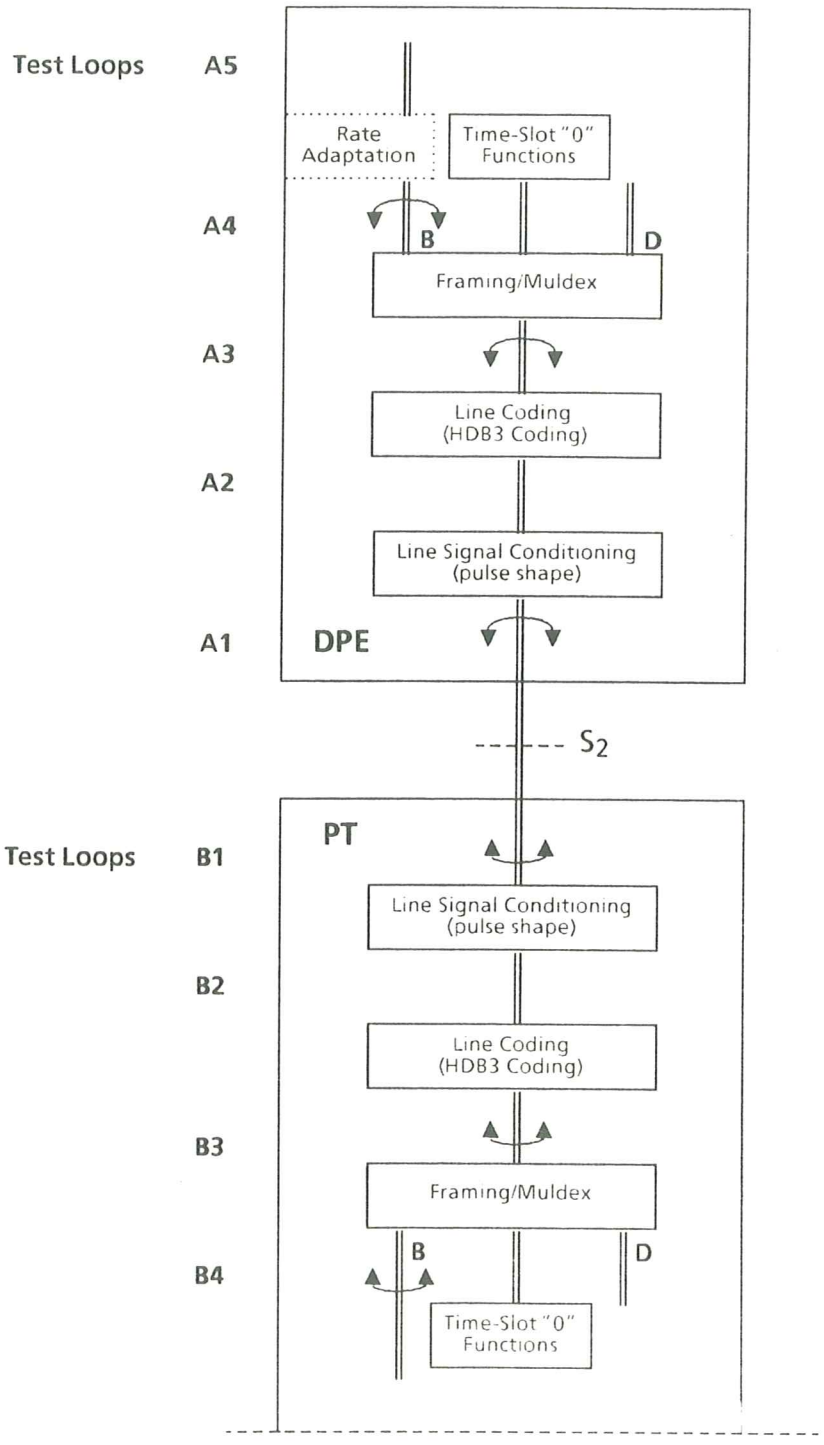


Figure 9 - Test Loops at the DPE and at the PT of a PCSN

Loop A1 is optional. When it is provided, it shall loop back any bit pattern received directly at the S_2 interface (ie. the pulse shape, see CCITT Recommendation G.703, is not

regenerated; this should be taken into account when using this loop for measurement purposes). If loop A1 can be activated via the S_2 interface, provisions shall be taken to allow also its deactivation, eg. by means of a timer.

Loop A3 is optional. When it is provided, it shall loop back any bit pattern received between its line coding functions (HDB3, see 7.5) and its framing/muldex functions. When loop A3 can be activated via the S_2 interface, provisions shall be taken to allow also its deactivation, eg. by means of a timer.

Loop A4 provides a loop back of any number of the 30 individual B-channels towards the PCSN. The loop shall preserve octet sequence integrity. It shall reflect any bit pattern received at the earliest possible time.

Loop B1 Whether or not Loop B1 is provided, depends on the implementation of the specific PCSN. When provided, it will loop back any bit pattern received directly at the S_2 interface (ie. the pulse shape, see CCITT Recommendation G.703, is not regenerated; this should be taken into account when using this loop for measurement purposes). When activated via the S_2 interface, provisions shall be taken to allow also its deactivation, eg. by means of a timer.

Loop B3 Whether or not Loop B3 is provided, depends on the implementation of the specific PCSN. When it is provided, it will loop back any bit pattern received between its line coding functions (HDB3, see 7.5) and its framing/muldex functions. When loop B3 can be activated via the S_2 interface, provisions shall be taken to allow also its deactivation, eg. by means of a timer.

Loop B4 Whether or not Loop B4 is provided, depends on the implementation of the specific PCSN. When provided, it will loop back any number of the 30 individual B-channels towards the DPE. The loop shall preserve octet sequence integrity. It shall reflect any bit pattern received at the earliest possible time.

9.2 Management Entity Primitives

The test loops shall be activated and deactivated by the Management Entity by means of the primitives:

MPH-LAR	MPH-LOOP ACTIVATION REQUEST	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.
MPH-LDR	MPH-LOOP DEACTIVATION REQUEST	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.

The activated or deactivated state of the loop(s) shall be indicated to the Management Entity by means of the primitives:

MPH-LAI	MPH-LOOP ACTIVATION INDICATION	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.
MPH-LDI	MPH-LOOP DEACTIVATION INDICATION	: The parameters shall indicate the type of the loop and the channel(s), where appropriate.

10 Electrical Characteristics

Unless specified otherwise in this Standard, the electrical characteristics shall conform to CCITT Recommendation G.703.

11 Power Feeding and Earthing

11.1 Power Feeding

No power feeding is provided via the S_2 interface.

11.2 Earthing

The PCSN will provide an earth connection via the S_2 interface. The DPE may use this PCSN-provided earth potential for its shielding. However, it must not interconnect this earth potential with any DPE provided earth potential (eg. that of the mains earth). See Figures 10 and 11.

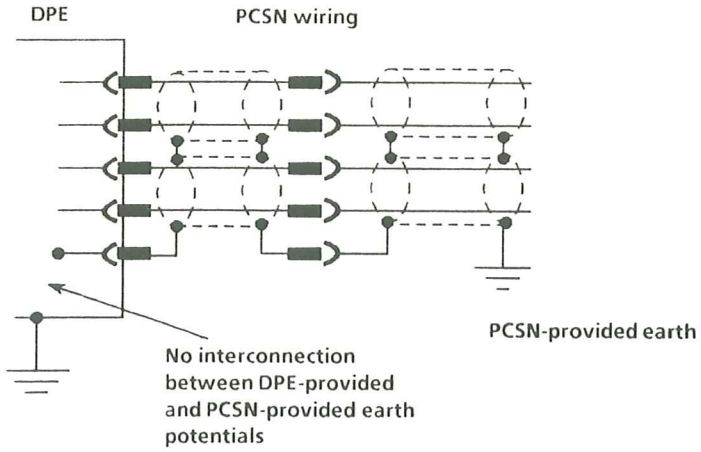


Figure 10 - DPE with its own Earth

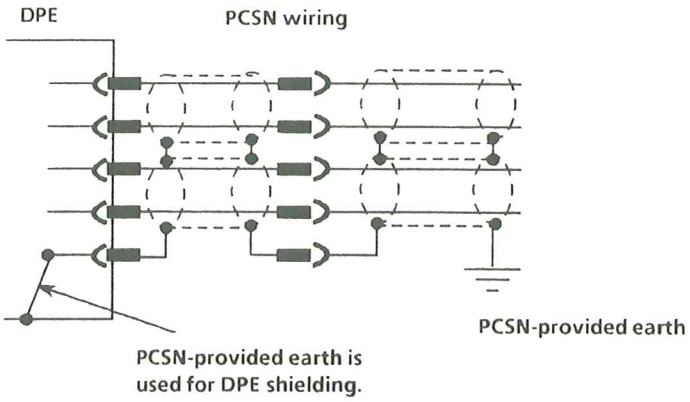


Figure 11 - DPE without an Earth of its own

12 Physical Characteristics

12.1 Connectors

The connectors remain to be specified. The specification shall comply with the requirements listed in Appendix B.

12.2 Connection Cords

The connection cords are considered to be part of the PCSN wiring. They will consist of two twisted and separately shielded pairs.

APPENDIX A

ACRONYMS

AMI	Alternate Mark Inversion
DPE	Data Processing Equipment
HDB3	High Density Bipolar 3
IWU	Interworking Unit
MPH-AI	Management/Physical Layer-Activate Indication
MPH-DI	Management/Physical Layer-Deactivate Indication
MPH-EI	Management/Physical Layer Error Indication
MPH-LAI	Management/Physical Layer Loop Activation Indication
MPH-LDI	Management/Physical Layer Loop Deactivation Indication
MPH-LAR	Management/Physical Layer Loop Activation Request
MPH-LDR	Management/Physical Layer Loop Deactivation Request
MULDEX	Multiplexer/Demultiplexer
PCSN	Private Circuit Switching Network
PH-AI	Physical Layer-Activate Indication
PH-DI	Physical Layer-Deactivate Indication
PT	PCSN Termination at the S reference point
SDL	Specification and Description Language
TE	Terminal Equipment

Appendix B: ECMA Requirements for the S_2 Connector

Connector Characteristics	Values Requested	Priority
Number of Contacts	• 4 excluding earth • an additional contact to convey PCSN earth	1 1
Fixed Connector	• female connectors for panel mounting	1
Free Connector	• male connector • female connector	1 3
Wiring on free Connector	• Flexible cable with 2x2 + 1 conductors	1
Type of cable	• twisted and separately shielded pairs for primary rate access	1
Cable strain relief		1
Bend protection		3
Maximum frequency	3 MHz	1
Bit rate	2 Mbit/s	1
Max. capacity between adjacent contacts	10 (...20 pF, see ECMA comments on transmission)	1
Expected number of operations for the free and the panel mounted connector	1000 insertions and withdrawals	1
Compatibility with existing connectors	• must not already be in use for applications which might impose a danger to the user (eg. with voltages above 42 V)	1
Coding	• the design should allow to be keyed as to prevent insertion into a wrong interface, eg. basic /primary rate access	1
Size of free connector	• minimum projection beyond mounting surface when mated with fixed connector	2
Easy to connect and disconnect	without tools	1
Polarisation	yes	1
Blind insertion	yes; with positive indication of latching	3
Non discriminative licences	• If patents exist for the connector, they must be offered to everybody on a non-discriminative basis at reasonable terms and conditions	1
Patents	• No patents/licences at all	3

1 = must be fulfilled.
2 = highly desirable; may only be missed, if contradictory to an item with priority "1".
3 = desirable.

ECMA Comments on Transmission Aspects of the Connectors at the Primary Rate (2 Mbit/s) Interface between Data Processing Equiment (DPE) and Private Circuit Switching Networks (PCSN)

1. The *attenuation* and the *return loss (ie. impedance matching)* of the connector are considered negligible in comparision to that of the cabling.

2. *Crosstalk* between the 4 signal contacts is of major concern. It depends on the pin allocation and on the capacity between adjacent pins.

   In order to minimize crosstalk, the pins should be allocated appropriately.

   - If **arranged in one line**, an appropriate arrangement could be, eg.

     SS E RR

     In contrast, arrangements like

     SRSR E or SSRR E

     should be avoided.

     (S= sender; R = receiver; E = Earth)

   - If **arranged at opposite sides of a knife-like plug**, the "knife" should serve as a shield between R- and S-leads by means of an interior heart made from metallic material.

     This interior shield should be connected to the earth contact provided by the PCSN at its S reference point to its DPEs.

   The latter arrangement promises to provide a better protection against crosstalk than the one-line arrangement.

3. ECMA considers an *upper frequency* of 3 MHz for the bandwidth as sufficient. If an appropriate pin allocation is defined, the capacity between adjacent pins could be up to 20 pF.